Journal of Electrical Engineering and Automation (ISSN: 2582-3051)
www.irojournals.com/iroeea/

A Performance Analysis of Switched Capacitor Based Multilevel Inverter

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Abstract

A multilayer inverter based on Switched Capacitors (SC) using the Nearest Level Modulation (NLM) technique has been presented. To generate five levels, this multilevel inverter employs eight switches and two capacitors. The technique of nearest level modulation is used to provide a high-quality output voltage with low harmonic content. According to the simulation results, the expected inverter has lower Total Harmonic Distortion (THD) than a conventional inverter, using a voltage balancing control mechanism. The voltage on the DC-link capacitor is balanced using the NLM method. Through a SC-based inverter in the NLM approach, different voltage levels can be produced with a high voltage gain, resulting in less power outages, less turning stress, and better converter efficiency. As a result, no further devices are required to balance the voltage of both capacitors. The proposed system is simulated with MATLAB/SIMULINK, and its THD performance is tracked.

Keywords: Switched Capacitor (SC), Nearest Level Modulation (NLM), Total Harmonic Distortion (THD), Multilevel Inverter, Cascaded H-bridge Inverter

1. Introduction

Multilevel inverters have been hailed as a viable solution for the most efficient electric power electronic conversion systems by both the scientific and industrial worlds. Motor drives, and locomotives all use multilevel inverters [1]. Their intrinsic properties, such as decreased dv/dt, high-quality output waveform, lower switching frequency, and so on, are the main reasons for their use. The cascaded H-bridge, neutral point clamped, and flying capacitor inverters are the most prevalent MLIs [2].

DOI: https://doi.org/10.36548/jeea.2022.1.003
Received: 14.03.2022, received in revised form: 09.04.2022, accepted: 15.04.2022, published: 26.04.2022

1.1 SC Topology

Several novel MLI topologies with lower component counts have been presented to address the aforementioned issue [3]. SC-based MLIs, on the other hand, are becoming increasingly popular [4]. While the majority of SCMLIs are buck, boosting circuits are required in systems driven by solar photovoltaics, fuel cells, or electric car batteries [5]. Furthermore, the necessity for an external boosting circuit is reduced by employing a switched capacitor in series/parallel with the input voltage source, resulting in a simpler circuit [6]-[8].

Several MLIs for a higher number of voltage levels have been described in the literature, leveraging the SC design, in an effort to develop a structure with the fewest number of components possible. Only one dc supply and eight switches are required for a five-level inverter in [9]. The authors of [10] created a circuit using eight switches, two capacitors, and a voltage gain of two in order to create a cost-effective architecture. Therefore, still requires two switches rated for peak output voltage due to the two capacitors, and it has a greater total stored energy. This research proposes a boosting factor- based 5 Level Switched Capacitor-based inverter.

The following are some of its most notable characteristics:

1) There are a total of eight switches that must be used.
2) The ability to reverse polarity.
3) Only switched capacitors must be intrinsically balanced; no sensors or complicated control methods are required.
4) Because four of the eight switches only run once every half-cycle, switching losses are reduced.

The functioning of the proposed topology as well as the related nearest level modulation (NLM) technique are thoroughly detailed. Experiments are carried out to confirm the accuracy, and the findings are reported for both steady-state and transient periods.

The benefits of the suggested topology over existing solutions are demonstrated through a detailed comparative study. The NLM is one of the organisations that uses it.

1.2 NLM Strategy

The MLI is driven with a low switching frequency using NLM. The sine wave component is the foundation of NLM's operation. The MLI output may be synchronised with a sine waveform using this method. The voltage magnitude of all the voltage sources in the symmetric setup is the same. The NLM technique changes the number of implanted sub-modules in the upper and lower arms at various stages to make the MMC output voltage closer to the modulation waveform, and it shows the relevant sub-module switching circumstances. When the output voltage level varies, this is the angle that changes. The amplitude of the modulation waveform is vm, and x is 0.5, indicating that NPA or NNA are rounded down to the next integer if the decimal fraction is less than 0.5, and up to the next integer if the decimal fraction is more than 0.5. The output voltage waveform's step number is N+1. When a consequence, as the number of series-connected sub-modules rises, the THD of output waveforms improves significantly, and it's simple to use when combined with the voltage balancing management approach and ranking strategy. [8] presents a modified approach in which the value of x (x=0.25) is changed to enhance output quality in low-voltage circumstances, and the output waveform's step number is increased to 9, as shown in Figure 4. Despite the lower THD of the output phase voltage, the average capacitor voltages of each sub- module fluctuate dramatically, and the switching frequency is substantially higher than with the traditional technique. [10] examines the modulation and step waveform areas at various time epochs and finds that when the last step sub-modules are put into arms, the inaccuracy is highest. It explains how to calculate a right time approach in order to minimise the inaccuracy. However, the generated waveforms are of lower quality than the original waveform analysis.

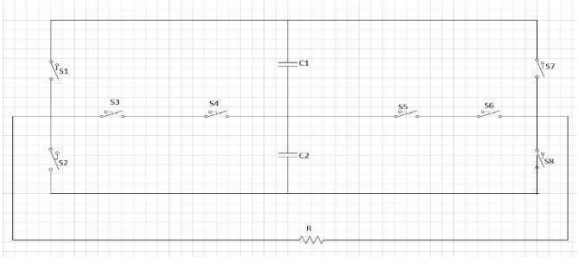

Figure 1. The SC inverter's circuit topology

A suggested SC multilevel inverter [12] is made up of two structures: a Sc circuit and a two- level inverter. Capacitors with switching devices such as MOSFETs and IGBTs make

up a switched capacitor topology. One capacitor and two switching devices operate one basic Sc cell. The Marx inverter circuit employed here is sometimes referred to as a Sc circuit. The capacitors Ck (k = 1, 2,... 2n 1) are swapped in series and parallel in these devices. The inverter bridge is made up of switches S1 through S4. The input voltage source is a voltage source Vin.

The inverter differs from traditional conventional inverter in that it is more basic. The proposed inverter lacks inductors, resulting in a massive system. This is a mixture of capacitors and alternative dc voltage sources that might be utilised as voltage sources for the inverter that has been mentioned [13]. As a result, the inverter may be used in grid-connected solar systems, among other things.

The suggested switched capacitor multilayer inverter's number of capacitors is given by,

$$ck = 2n – 1$$

The number of switched-capacitor cells in the system is denoted by n. The suggested inverter's output voltage waveform is (4n-1) levels.

Table 1. Comparison of devices for changing

	Leveling	**Diode clamped**	**Flying capacitor**	**Conventional**	**SC**
Switching Devices	5 Level	12	12	8	8
	11 Level	20	2	20	16

The proposed inverter requires fewer components than a traditional cascaded multilevel inverter of the same configuration. Table I compares the number of switching devices utilised in various types of multilevel inverters.

2. Multilevel Inverter

Figure 2 depicts the newly created proposed multilayer inverter. In comparison to other conventional approaches, the suggested inverter uses fewer switches. The submodule arrangement is used to design this inverter. Each submodule has four switches and two DC

link capacitors. Depending on how many levels there are, submodules will be added to the inverter.

This inverter only requires one isolated DC supply. m=2S+1 is the multi - layer perceptron. The number of submodules is denoted by S. In this situation, we'll need two input stages (Vdc and 2Vdc). As a result, we'll need two submodules to make five levels. To produce 5 levels, this suggested inverter requires eight switches and two link capacitors. The four switches are located in the submodules, and another four switches are utilised to generate an AC signal by switching the positive and negative cycle.

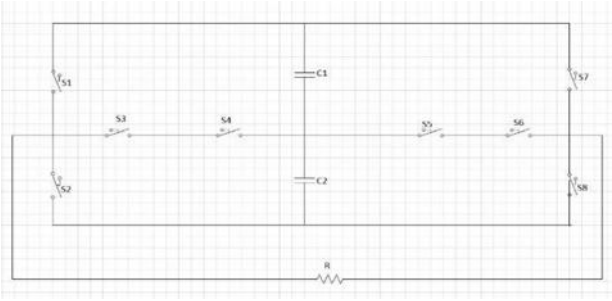

Figure 2. Block diagram of the suggested system

The block diagram of a SC based multilevel inverter employing the NLM technique is shown in Figure 4. The multilayer inverter helps in DC to AC conversion. The multilayer inverter switches are triggered using the NLM method. After the DC to AC conversion, the filter aids in the reduction of harmonics.

Instead of standard two/three-level inverters, the best power electronics converters for producing high-quality ac waveforms are multilayer inverters. However, the modulation method used by the multilayer inverter has a significant impact on the ac power quality. As a response, the simulation is conducted using the recommended NLM approach in MATLAB/Simulink, and the results are given. In compared to the classic NLM system, the NLM approach reduced voltage THD and improved sub-U MLI characteristics.

The NLM technique for most reduced switching frequentative balancing algorithm [28] is depicted in Fig. The inserted submodule calculates the upper and lower arm members.

$$\text{Udc} = \{most\} 2\text{Ud}$$

$$NL = round0.5\ \{Udc\ [1+mcos(\omega t)\}$$

The round function (round0.5 (x)) utilizes the decimal fraction of x to round the real value x to the nearest. If the decimal fraction of x is higher than 0.5, it is rounded to the next whole number; otherwise, it is rounded to the next whole number. The operation principles of the NLM techniques are shown in the below figure, using a multimodule control (MMC) with 10 sub - modules per arm.

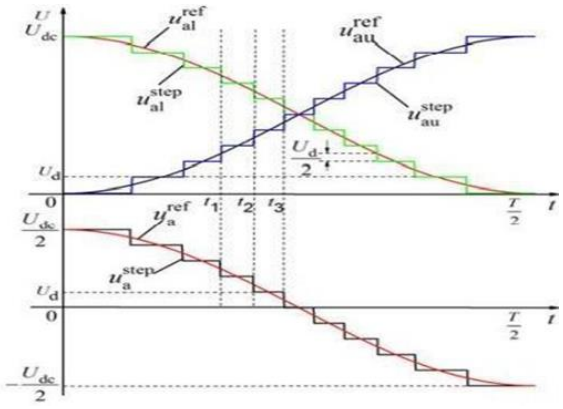

Figure 3. The NLM method's principles

Two cases [t1 to t2, t2 to t3 in Fig.] are examined to better grasp the principle of the traditional NLM approach.

$$ULref = (M+0.5)Ud$$

The arm voltages and ac EMF step waves are provided as urefL =[(M1)+0] in the first example Ud urefe = (M0.5N0.5) Ud urefe = (M0.5N) Ud urefe = (M0.5N) Ud

The second scenario is from time t2 to time t3. ustepL =(M1) may be used to show the arm voltages and ac EMF reference values at t = t2.

Because the positive and negative dc voltage constraints are 0.5Udc, the maximum level number in ac EMF is equal to Udc/Ud + 1 (i.e., N + 1). When shifting steps, the maximum error between uref e and ustep shows (i.e., t1, t2, and t3).

2.1 Operating Principle

This research proposes a five-level switching capacitor based multilevel inverter. The structure of a 5 Sc multilevel inverter is shown in Figure 2. By switching the capacitors in

series and in parallel, the proposed inverter provides a multilayer ac voltage that is greater than the input dc voltage. The capacitors are charged when the capacitor as well as, as well as the input

Voltage supply, the input voltage supply is linked in parallel. The capacitors are discharged when the capacitor and the voltage level supply are connected in series. NLM methods are used to create the gating signals for the circuit's switching components. They proposed inverter's (5- level) operation can be demonstrated in five states: once all capacitors are coupled in parallel, one capacitor in series, and another capacitor in sequence. Using the modulation technique, the gate-source voltage is used to drive the switches. The following is a table of switching states.

Table 2. The list of state switches in each state

Switches	+2V	+V	0V	-V	-2V
S1	OFF	OFF	ON	ON	ON
S2	ON	OFF	OFF	OFF	OFF
S3	OFF	ON	OFF	OFF	OFF
S4	OFF	ON	OFF	OFF	OFF
S5	OFF	OFF	OFF	ON	OFF
S6	OFF	OFF	OFF	ON	OFF
S7	ON	ON	ON	OFF	OFF
S8	OFF	OFF	OFF	OFF	ON

3. Simulation Results

Cascaded H Bridges, null clamp, and capacitors multilevel inverters are the most prevalent topologies. A switching capacitor-based multilevel inverter with fewer switches was modelled using MATLAB-Simulink. The R load is expected to be fed by the switching capacitor-based multilevel inverters. The results are compared to a typical conventional inverter under the identical load conditions. The NLM seems to have a carrier frequency of

2.5 kHz and a 50 Hz output frequency. The output voltage peaks at approximately 300V, confirming the higher voltage gain of the recommended topology's 200V input voltage.

In order to increase the input voltage. Under various loading situations, the capacitor voltages in both cases remained at 100V, demonstrating that the capacitor voltages C1 and C2 are self-voltage balanced. Changes in modulation index, as well as variations in load parameters, have been modelled for the proposed five-level architecture. The impact of altering

The MI on the output voltage can be seen in Figure 10, where the output voltage's Computed value is 206.5 V. The MI is changed to 0.5 in 0.35 seconds, reducing the number of levels from nine to five and lowering the RMS value to 146.3V. It can be made using any of the above-mentioned nearest level modulation approaches. The output voltage of the proposed switched capacitor multilevel inverter can be seen in Figure 10. Figure 11 shows the THD of the output voltage utilizing next level modulation strategies in comparison to the standard cascaded H-bridge inverter topologies in Figure 7.

3.1 Inverter with Multiple Levels (Conventional)

To produce the 5-level output voltage, the tumbled bridge multilevel inverter has two Dc voltage sources and 8 bidirectional switches. Figure 4 depicts the 5-level cascaded H bridge MLI of Simulink, whereas figures 6 and 5 depict the output of voltage and subsystem diagrams, respectively. The output voltage levels are determined by the number of sources and switches used. As a result, this method takes up more space and creates a more complicated circuit. Figure 7 depicts the waveform's complete harmonic distortion spectrum.

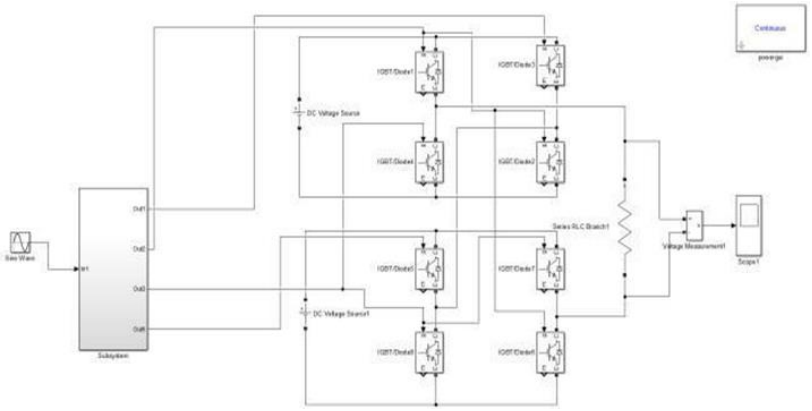

Figure 4. The typical multilayer inverter's main system

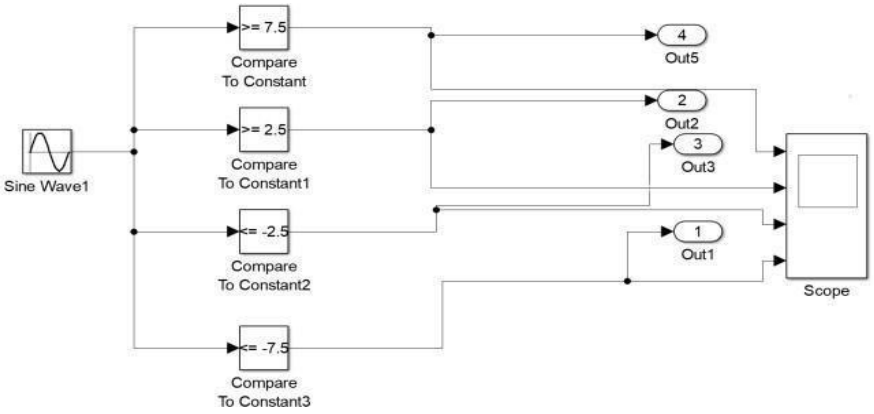

Figure 5. The standard multilevel inverter's subsystem.

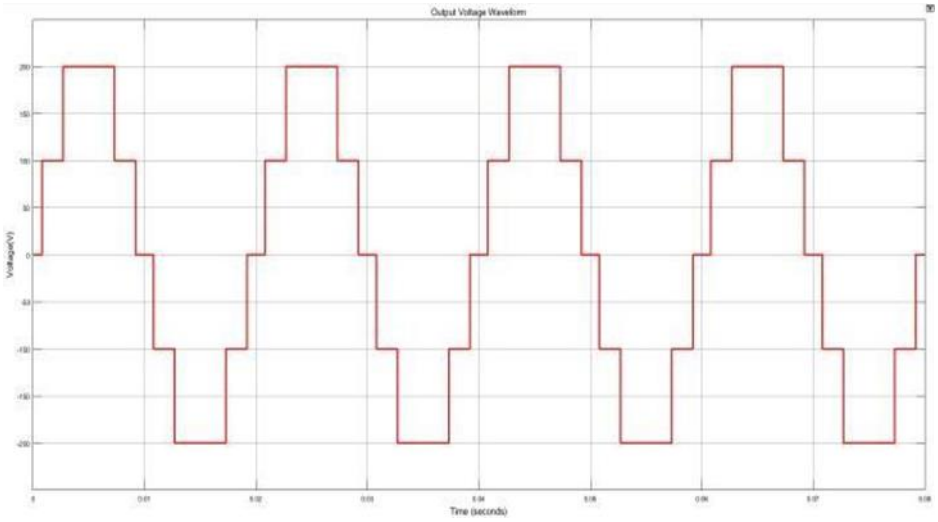

Figure 6. The traditional multilayer inverter's output voltage

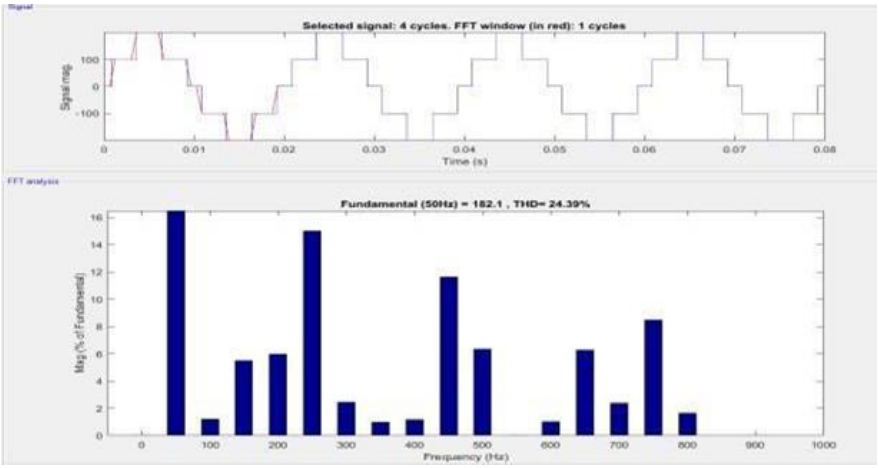

Figure 7. The suggested multilayer inverter's Total Harmonic Distortion (THD)

3.2 Proposed Multilevel Inverter

Figure 8 illustrates the Simulink diagram's suggested structure. An only DC supply and six bidirectional switches are present. The switch settings must be complementary to prevent DC

Voltage sources from being short-circuited. The number of switches decides the number of levels. The output voltage is enhanced by the capacitor. Figures 10 and 9 show the voltage waveform's output and the subsystem diagram, respectively. The switching capacitor based MLI has a total harmonic distortion of 17.66 percent.

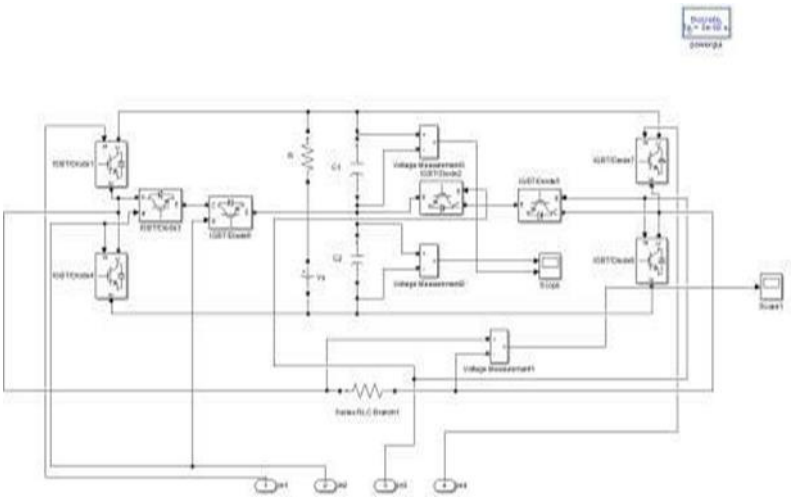

Figure 8. The suggested multilayer inverter's main system

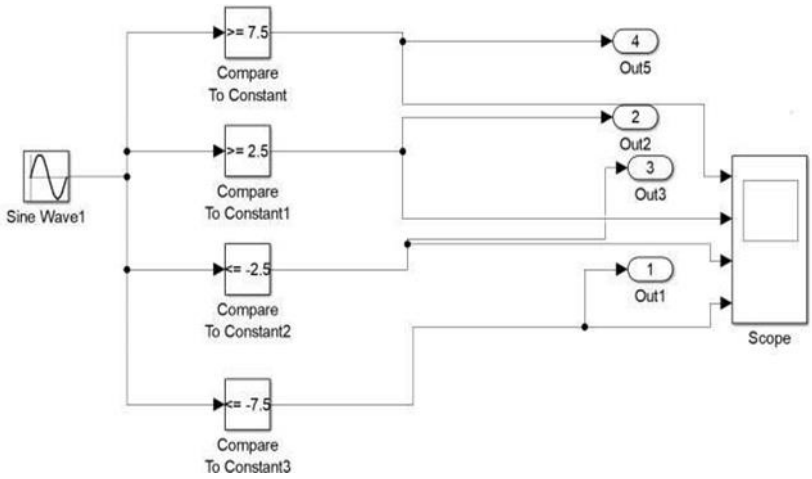

Figure 9. The suggested multilayer inverter's subsystem

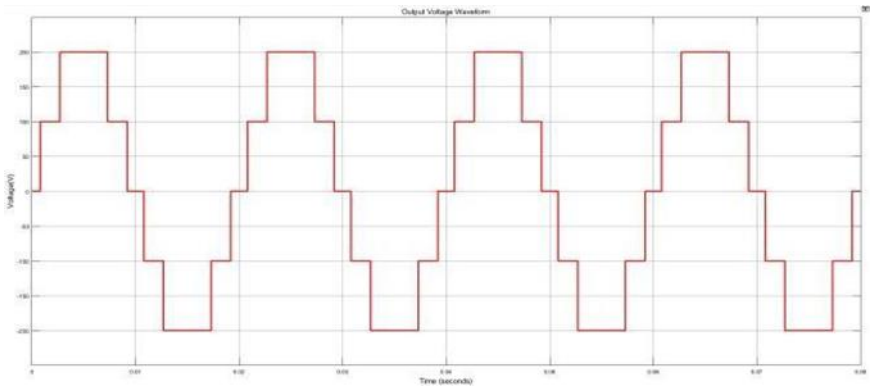

Figure 10. The suggested inverter's output voltage

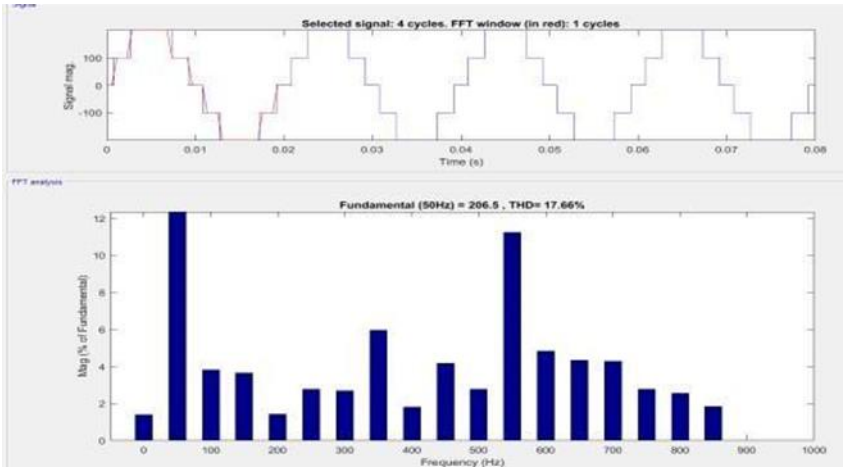

Figure 11. The proposed multilayer inverter's THD

Table 3. THD comparison of conventional and preliminary multilevel converter

Five Level Converter	Conventional Converter	Switched Capacitor based Converter
Switches Used	8	8
Voltage Source(V)	200V	200V
Number Of DC Source	Two	One
Resistive Load	100 ohms	100 ohms
THD Value by NLM Method	10.47%	5.2%

MLI's output voltage has some harmonics in it. The input voltage in the above two configurations is 200V, and the load is resistive. When compared to standard 5 levels of MLI, a switched capacitor-based MLI reduces THD by 4.8 percent. The suggested inverter, according to the research, has a lower THD than a typical cascaded multilayer inverter. The resultant THD should decrease as the number of resulted in the high.

4. Conclusion

For a SC-based multilevel inverter, the nearest modulation technique is employed in this project. The switch capacitor-based Multilevel Converter architecture has been found to yield less Total Harmonic Distortion. When the Nearest Level Modulation control technique is combined with this multilayer topology. A Sc-based multilevel inverter is compared to a H- bridge multilevel inverter in terms of performance. There is evidence that a Sc-based multilevel inverter uses fewer switches and dc sources while outperforming cascaded H-bridge inverters. Through the use of a Sc-based multilayer architecture, harmonics are reduced. To comply with the IEEE harmonics requirement, passive filters will be built and coupled to the output of the Sc-based multilevel inverter.

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