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Design and Implementation of CMOS K-Band Phase Shifter using 90nm

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Abstract

We suggested designing a 24 GHz K band CMOS phase shifter using 90nm technology in this paper to satisfy the need for integrated and high-performance components for wireless system development. For the best phase shift and the least amount of insertion loss, the phase shifter operates between 18 and 27 GHz using a combination of lumped and distributed components. Important considerations are phase selectivity, linearity, and impedance matching. Theory and experiments demonstrate that it has a 180° range of phase shift and is utilized in high-frequency applications. The study demonstrates how 90nm CMOS technology can be used to improve wireless communication.

Keywords: Complementary Metal Oxide Semiconductor (CMOS), Radio Frequency Design, Root Mean Square (RMS)Gain Error, RMS Phase Error, Phase Shifter.

1 Introduction

High-speed, small, and efficient electronic devices are gaining significance in view of recent developments in wireless communication technology. Phase shifters play a critical role in beamforming, phased-array antennas, and signal processing systems, especially in the frequency range of K-band (18-27 GHz). They are also required in advanced radar systems, satellite communications, and [2] future 5G networks. Integrated and miniature phase shifters both work well at high frequencies.

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Phase shifters primarily utilize discrete passive elements or principal microwave technologies. With phase shifters being incorporated within CMOS technology, numerous advantages in terms of cost, size, and power consumption are achieved. The 90nm CMOS process technology has enabled high-speed, high-frequency circuit design to achieve a good balance between production capability and performance. Minimizing insertion loss [3], high isolation, and accurate phase shifting are challenges in the absence of these advantages. Sophisticated design techniques such as impedance matching, dynamic range optimization, and calibration are key to overcoming these challenges. The inherent parasitic capacitances and inductances of the CMOS technology need to be closely monitored to preserve maximum efficiency at K-band frequencies. It is possible to achieve precise phase control with minimal signal loss by utilizing lumped and distributed components together.

The implementation and design of a 90nm technology-based K-band CMOS phase shifter are extensively discussed in this study. The effective implementation of a phase shifter aids in design of stable, compact, and efficient RF components, and thus verifying that CMOS can be applied to high frequencies. These developments are critical for improving functionality and securing the integration of next-generation communication networks by reducing size and power consumption, and meeting the requirements of high-rate wireless networks.

2 Literature Survey

The development of CMOS-based phase shifters for high-frequency purposes, especially in the K-band (18-27 GHz), has been the focus of extensive research in recent years. The CMOS technology is a useful method because of its low cost, scalability, and strong integration capabilities. Although K-band performance is still challenging, phase shifters at microwave and millimeter-wave frequencies have been part of several studies.

Based on a 4x1 beamformer IC, this research [1] designed a multiband phased-array module that supports 5G NR FR2 standards and operates between 15 and 57 GHz. The requirement for multi-standard, multi-band communication modules is met by such wide frequency coverage and reconfigurability, resulting in application variation. For mmWave systems, high-power PAs are necessary for attaining long-range transmission. A three-stacked CMOS PA was introduced by this system [2]. It offers improved power and thermal/electrical durability and is designed with mmWave beamforming systems in consideration.

A K-band PA with 180° phase-shift capability was developed using a low-power CMOS method [3] and a K-band LNA with an integrated 180° phase shift function based on a cascode structure [4] are two significant works that the research presented. These innovations make it possible for beamforming topologies to include more functional and compact front-end components. A small Ka-band 4-bit phase shifter that has minimal group delay variation was invented by this research work [5]. A statistical digital predistortion (DPD) technique was proposed in this research [6] for reducing random amplitude fluctuations in 5G mmWave RF beamforming transmitters. The technique maintains signal integrity and is resilient to work under poor operating conditions. A 275–320 GHz reflection-type phase shifter was described in this research [7], introducing CMOS-based solutions into the sub-terahertz range that can be used for radar and future 6G applications. For 5G applications, Lee et al. [8] introduced a multi-band reconfigurable differential power divider. The two most crucial features for flexible multi-band RF front-ends are their adjustable frequency modification and reduced signal degradation. A K/Ka/V tri-band receiver with a constant-gain phase shifter and variable-gain LNA in a single-signal-path design was introduced in this research [9]. The technique is made simpler and more integrated in multiband front-end systems since it is implemented in 28-nm CMOS. Li et al. [10] proposed a 60 GHz 5-bit phase shifter with an integrated variable gain amplifier (VGA) and phase-error modification for improved linearity and configurability under various situations. The research [11] proposed a low-insertion-loss and RMS-error 5-bit phase shifter designed for 5G in 65-nm CMOS. A 6-bit CMOS S-band phase shifter with improved resolution for increased beamforming granularity was proposed in this methodology [12]. The work [13] designed a tiny 5-bit passive phase shifter operating at 57–64 GHz that only occupies up to 0.094 mm^2 of chip space, making it ideal for dense phased-array integration. This research [14] focused on improvements in monolithic integration and area-efficient full-duplex communications systems, suggesting an X-band bi-directional phased-array T/R chipset in 0.13 μm CMOS. To minimize signal degradation, Shin et al. [15] used a switched capacitor technique to create a 4-bit low-insertion-loss phase shifter in 65 nm CMOS. A low-phase-error 5-bit passive phase shifter operating at 27–42 GHz was designed by Tsai et al. [16] with a focus on beam control precision and bandwidth. In fact, random fluctuations and nonlinearities pose a serious problem for mmWave systems.

The current study aims to overcome these problems by utilizing 90nm CMOS technology to create a low-loss, energy-efficient K-band phase shifter.

3 Existing Methodology

Before simulating a K-band CMOS phase shifter, it is essential first to establish performance goals such as phase shift range, frequency coverage (18-27 GHz), insertion loss, and return loss. Choosing the appropriate simulation tools is crucial. Circuit-level analysis is most effective using tools like Keysight ADS or Cadence SpectreRF, as they provide high-frequency effects and parasitics modeled with EM simulation tools like ANSYS HFSS or Keysight EMPro to ensure precise performance evaluation. Circuit schematic diagrams are developed, DC and AC studies are performed, and nonlinear behavior is evaluated using harmonic balance or transient analysis as part of the simulation process. Parasitic interactions are then modeled using EM simulations. The design is improved by optimizing component values and arrangement based on the combined results of the two simulations. This continuous procedure ensures that the phase shifter achieves the performance requirements before manufacturing.

A 5-bit K-band CMOS switch-type phase shifter with an L-C-L T-type low-pass structure is used in an existing system. Accurate phase control with minimal insertion loss is achieved by the system through the optimization of the resonance frequencies of inductors and capacitors. To save chip space and minimize insertion loss, the 180° bit is not included in the design. If a 180° phase shift is required, a differential amplifier is used. The phase shifter is made using 65nm CMOS technology, which has an insertion loss of 7.44 ± 2.0 dB, a Root Mean Square phase error of 2.6°, and a Root Mean Square gain error of 1.2 dB. It operates between 22.0 GHz and 23.0 GHz. Narrow operational bandwidth, comparatively high insertion loss, and dependence on precise EM simulations are some of the drawbacks of the current architecture. When integrating using differential amplifiers, avoiding the 180° bit can complicate the design. Furthermore, real-world performance may be impacted by parasitic effects and the restricted scalability of higher-bit phase shifters. Developing phase shifter designs for complex communication systems require addressing such problems.

4 Proposed Methodology

4.1 Proposed Design Technique for the T-Type Phase Shifter

The phase shifter in the present study contains five control bits, with the exception of the 180° bit. In general, implementing the 180° bit in a phase shifter reduces the working bandwidth, increases insertion loss, and requires more chip space than other bits. A practical

technique to achieve the 180° phase shift is to use a differential amplifier arrangement. This method maintains a wider bandwidth, minimizes insertion loss, and reduces the size of the device. For instance, differential designs can be used to incorporate the 180° phase shift into power amplifiers or low-noise amplifiers. Thus, the 180° bit was removed from this study's phase shifter design.

Figure 1 illustrates the L-C-L T-type low-pass filter configuration used in the unit-bit design. The structure of all five bits (5.625° to 90°) is the same. For pass and shift modes, transistor M1 alternates between ON and OFF states, whereas transistor M2 operates opposite to M1 to ensure balanced functioning. The parasitic components of M2 are shown by RM2 and CM2, whereas the parasitic resistance of M1 in the ON state is represented by RM1. The terminal impedance is assumed to be 50 Ω for analysis, with capacitance modeling in the OFF state and minimal resistance in the ON state. EM simulations are used to improve the final component values for accuracy.

4.2 Assumption and Simplification for Analysis

A CMOS switch-type phase shifter with an L-C-L T-type low-pass filter configuration is seen in Figure 1. Phase shifting is the function of transistor M1, and complementary switching is provided by transistor M2. The phase shift is determined by the capacitor CSHC_{SH}CSH, the inductors LSHL_{SH}LSH, and the LREL_{RE}LRE. For precise phase corrections, the transistor states are regulated by the control [7] voltages VCV_CVC and VCOV_{CO}VCO.

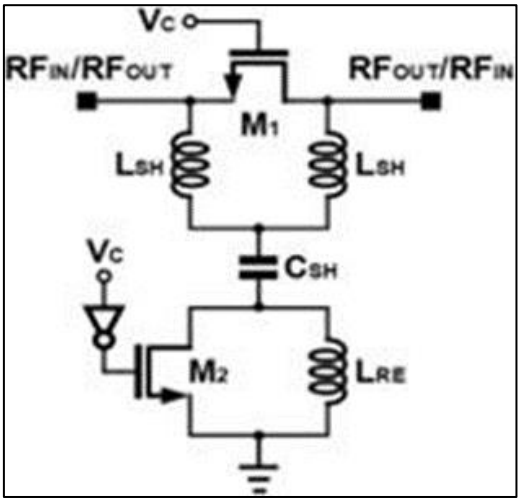

Figure 1. Diagram of Proposed Technique T-type Structure

4.3 Operation Analysis

Shift mode: The resistance of RM2 is considered to be insignificant in the shift mode functioning of a CMOS phase shifter compared to the reactance of the shunt capacitor (CSH) and the series inductor (LRE). Thus, as seen in Figure 2, the circuit may be reduced to a T-network made up of LSH, CSH, and LSH. The analysis first excludes the parasitic capacitance of transistor M1M_1M1 in its OFF state to simplify it. However, the overall design efficiency is improved by lowering the necessary LSHL_{SH}LSH by including this capacitance in the final optimization [11] procedure.

Overall Design Flow Chart

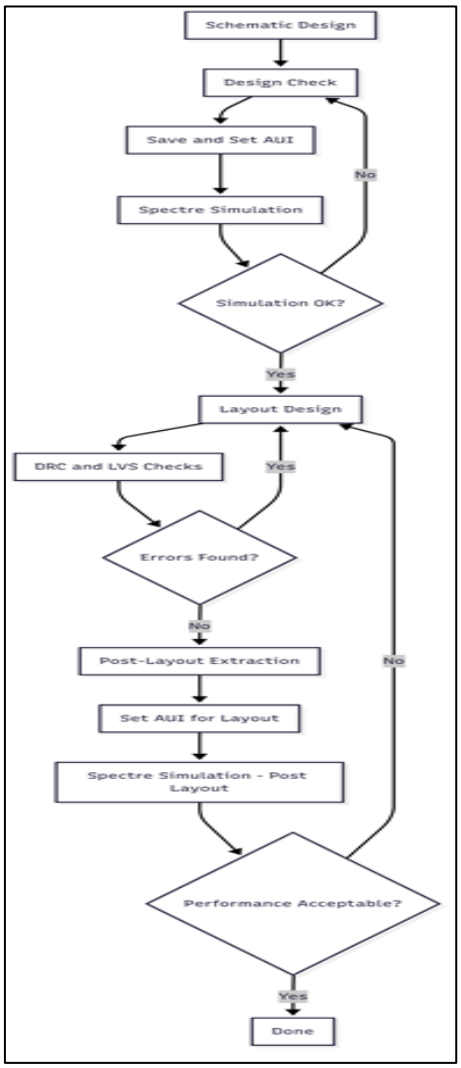

Figure 2. Flow Chart

Pass Mode: The following figure 2 shows how the circuit's analogous behavior varies with frequency in pass mode. Using the circuit in [16], the equivalent impedance,

ZEQZ_{EQ}ZEQ using this mode the given information will perform well across the frequency range.

This flowchart diagram 2 illustrates that the integrated circuit (IC) design and verification process begins with schematic design and on to layout design and simulation. The first circuit is created at the schematic design phase of the process. After that, the design is stored and error-checked. Before continuing the design, discovered errors must be fixed. If no errors are found, the design is set up [2] using the Analog Design Environment (ADE) to evaluate the design's functionality using Spectre simulation. The method proceeds if the simulation indicates that the design satisfies the requirements; if not, it goes back to the schematic design stage for revisions.

Layout design is the next step once the requirements for schematic design are completed. Design Rule Check (DRC) is used to verify that the layout meets the manufacturing requirements. If errors are identified, they must be corrected. The design is extracted to provide a netlist that indicates the layout if the DRC is accurate. Layout vs. Schematic (LVS) is then used to compare this netlist to the schematic. Corrections are made if LVS finds differences; if not, the design is established in ADE [8] and goes through Spectre simulation. The design is considered complete if the simulation satisfies the performance criteria. If not, the layout design is modified, and the procedure is repeated until all requirements are met.

Software Used: According to the description supplied, Cadence Virtuoso is a complete IC design suite that is frequently used for IC design and simulation, particularly for analog, mixed-signal, and radio frequency designs. Virtuoso provides a comprehensive design platform that includes features such as schematic capture, which enables engineers to design circuits visually, and simulation, which allows them to examine the circuit performance in various scenarios, including noise, AC, DC, and transients. Additionally, the platform offers physical layout design tools to guarantee that the location of components on the chip precisely corresponds to the desired circuit performance.

Crucial verification techniques like Layout vs. Schematic (LVS), ensure that the physical layout corresponds with the schematic design, and Design Rule Checking (DRC) identifies possible manufacturing problems. These techniques are integrated into Virtuoso. The program is highly effective for creating high-performance, manufacturing-ready integrated circuits because it enables task automation and adaptable design procedures. Cadence Virtuoso

is a common tool in the semiconductor industry due to its complex features and adaptability that enable the design of complex devices used in a variety of applications, such as consumer electronics and telecommunications.

5 Results

5.1 Proposed Schematic Diagram

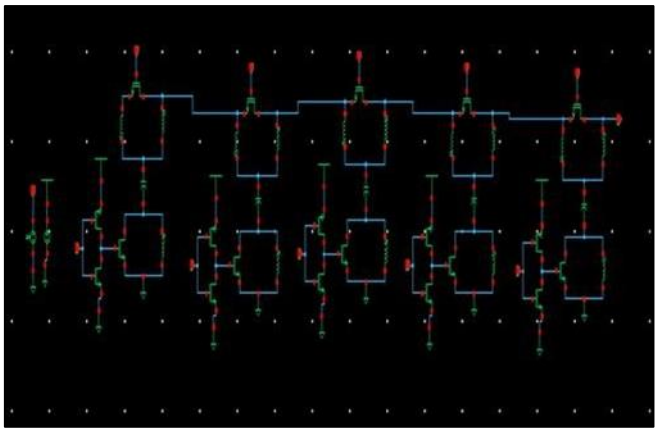

Figure 3. Screen shot of Schematic Diagram

The circuit diagram 3 displayed a multi-stage CMOS phase shifter that is apparently connected with users' K-band CMOS phase shifter work. In high-frequency circuits, cascaded differential pairs are commonly utilized to provide precise phase control. The use of LC tuning networks for phase shift control is indicated by the differential amplifiers, inductors, and capacitors per stage. The dynamic phase shift control via the control voltages is indicated by the many biasing points. This is typical of vector modulation circuits, where the signal may be accurately phase-controlled, and each stage adds an incremental phase shift.

Developing a wide range of phase shifts with less insertion loss is the primary goal while designing the CMOS phase shifter. Using differential pairs in conjunction with inductive and capacitive components helps achieve precise phase alterations for K-band applications (18–27 GHz), including 5G networks and phased arrays. While harmonic balance analysis is useful for evaluating non-linear phenomena, S-parameter simulations are required for the investigation of phase shift and insertion loss to validate the performance of this circuit.

Accurate implementation of biasing and matching is necessary when working with Cadence Virtuoso in order to preserve impedance as frequency varies. To remove unwanted effects and preserve stable phase at high frequencies, layout modification is also required. This

will help users with the simulation setup, design optimization for improved efficiency, or layout modification for K-band standards.

5.2 Proposed Wave Form

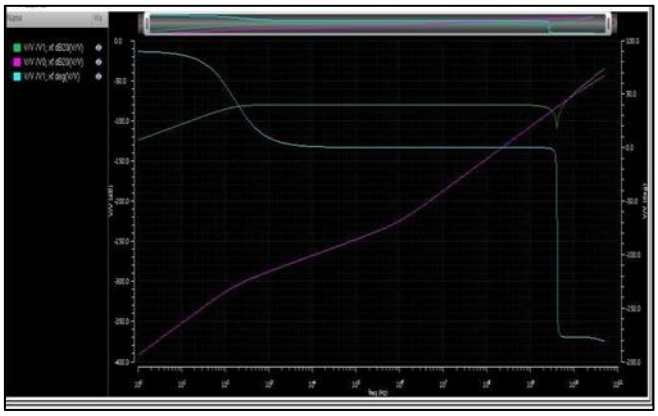

Figure 4. Screenshot Graph of Insertion loss

The proposed K-band CMOS phase shifter's frequency response is displayed in graph 4, where the x-axis represents frequency and the y-axis displays magnitude (dB) and phase (degrees). The various lines likely represent various bias voltages that regulate the phase shift. A phase curve that increases smoothly indicates that the circuit is altering the phase as it is expected. Phase shift range, insertion loss, and phase linearity are essential variables to examine. A 360° phase shift and an insertion loss of less than -10 dB are usually optimal for K-band (18-27 GHz). If performance needs to be improved, consider matching optimization, LC network modifications, or bias modification.

5.3 Designed Technique for Maximum Gain Error

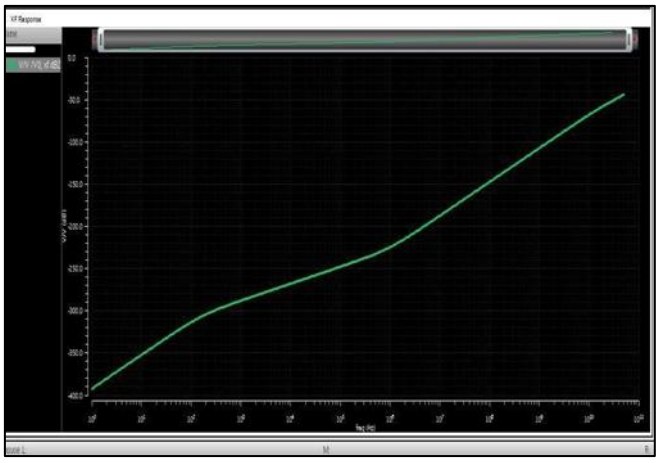

Figure 5. Screenshot Graph of Maximum Gain Error

The maximum gain error in the design and development of a 90nm CMOS K-band phase shifter is illustrated in Figure 5 above. With the x-axis representing frequency (Hz) and the y-axis representing gain, the pattern shows how gain changes (in dB) in relation to frequency. As the frequency increases, the pattern shows that the gain error decreases, which provides a necessary means to ensure dependable phase shifting for K-band activities (18–27 GHz). Optimizing phase shifter performance in high-frequency radar and communication systems depends on this work.

5.4 Designed Technique for Phase Error

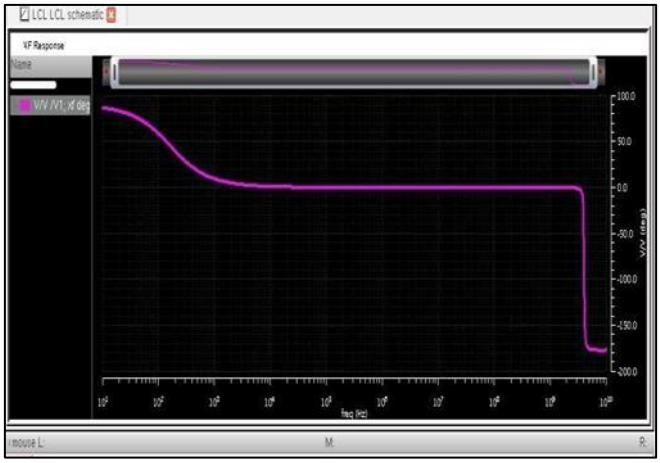

Figure 6. Screenshot Graph of Phase Error

Figure 6 presents the device's performance throughout the 18–27 GHz range and shows the phase shift fluctuation with frequency. A rapid drop-off at higher frequencies, a continuous phase shift in the operational bandwidth, and a gradual decrease at lower frequencies can all be observed in the displayed phase response curve. The measured phase error indicates departures from the ideal shift, that are reduced by the optimization of LCL architecture and appropriate impedance matching. For 5G beamforming, radar, and satellite communications applications, precise phase control is required to ensure effective signal direction and minimal distortion, making performance important.

5.5 MoS Count of Schematic Diagram

The K-band CMOS phase shifter was developed using 90nm process technology. Figure 7 shows the screenshot of MoS count. It is essential for advanced millimeter-wave and radio frequency communication systems because it allows for accurate phase adjustment for effective beamforming applications.

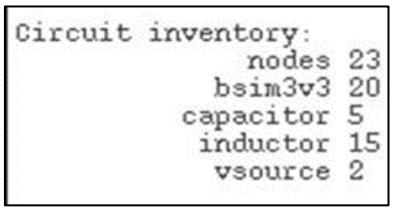

Figure 7. Screenshot of MoS Count

With 23 nodes, 20 BSIM3v3 MOSFETs, 5 capacitors, 15 inductors, and 2 voltage sources, the design inventory demonstrates a circuit complexity that combines active and passive components for the most effective phase shifting results. Phased array antennas, 5G communications, and radar applications will benefit from the compactness, low power consumption, and high frequency operation that 90nm CMOS technology offers.

6 Conclusion

This paper presents the design of a K-band CMOS phase shifter with an L-C-L T-type low-pass structure. Utilizing the L-C-L T-type structure's resonance properties, a novel design method was used to reduce RMS phase and gain errors. Each bit in the optimization process yielded two different resonance frequencies, which were then used to determine the phase shift. The design parameters were suitably changed to guarantee equal gains between the shift and pass modes for the intended use. To evaluate the effectiveness of the suggested method, a 5-bit K-band phase shifter was designed using 90 nm RFCMOS technology. With stable insertion loss and low RMS phase error and gain error, the results demonstrated consistent performance over the intended frequency range.

In order to improve the accuracy of EM simulation and lessen discrepancies between simulation and measurement results, future work on the K-band CMOS phase shifter will concentrate on improving the 90° bit design. Additionally, the adaptability of the design may be improved by employing a 180° bit while keeping it small and minimizing insertion loss. Increasing the operating bandwidth over the current 22–23 GHz range is another crucial strategy to cover a wider spectrum for satellite and 5G applications. Enhancing power management and efficiency can further boost performance, especially for communication and high-power radar systems. Investigating state-of-the-art CMOS technologies, like 22 nm or FinFETnodes, could lead to a smaller device, better linearity, and lower power consumption.

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