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High-Data-Retention 6T SRAM with Dual Sleep-Transistor Power-Gating and Duty-Cycle Aware Energy Analysis for Low-Power IoT Application

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Abstract

Static Random Access Memory (SRAM) is the main contributor to standby power dissipation in duty-cycled Internet of Things (IoT) systems. The paper presents a 6 transistor SRAM cell that has low leakage and dual sleep transistor-based power gating. The memory cell is mode aware and supports different modes of operation. The header PMOS and footer NMOS sleep transistors have been used to minimize leakage and retain stored information during extended periods of sleep. The proposed memory architecture is validated through 45 nm CMOS models and simulations in LT spice. The memory is able to achieve picoampere levels of supply current in deep sleep mode. A duty cycle aware analysis of energy dissipation is also presented. The analysis shows that the proposed memory is an effective solution for ultra-low-power memory in IoT systems.

Keywords: Low-Power SRAM, Dual Sleep Transistor, Power Gating, Data Retention, Deep Sleep Mode, IoT Applications, Leakage Reduction.

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1. Introduction

The rapid growth of IoT devices has created a need for the development of ultra-low-power digital systems that can operate over extended periods of time with extreme levels of energy constraints. Such applications include environmental monitoring, wearable electronics, smart healthcare, industrial sensing, etc., which rely on battery-powered or energy harvesting-based systems. In these types of systems, the static random access memory (SRAM) used plays a vital role as it consumes a considerable percentage of the total silicon area as well as the total power dissipated. In IoT-based systems, the workloads are of a duty-cycled nature, meaning there are extended intervals of inactivity between short, intermittent active intervals. Thus, reducing the SRAM leakage power while maintaining the data has become a serious challenge.

The conventional 6T SRAM circuits are popular due to their simplicity, high performance, and strong read-write behavior during active operation. However, in deep submicron CMOS technology, 6T SRAM circuits face critical issues with subthreshold leakage, gate leakage, and junction leakage current, especially during standby operation. As technology advances, the ratio of leakage current to active current becomes greater, and the ratio of leakage current to dynamic current becomes larger. As a result, the conventional SRAM circuits are no longer suitable for energy-constrained IoT devices. Although deep power gating techniques can minimize the leakage current by disconnecting the supply voltage, completely removing the supply voltage causes data loss, and the system must be reset during wake-up.

In order to reduce standby leakage and retain the data, several low-power SRAM techniques have been reported, including multi-threshold CMOS, sleep transistor, drowsy cache, and voltage scaling. Although these techniques show some level of leakage reduction, some of the techniques show some disadvantages, including decreased data stability, wake-up overhead, and limited scalability and flexibility. In addition, most of the existing works only consider the reduction of leakage current under a single standby condition without considering duty cycle-aware characteristics, which is common in IoT devices, as memory is frequently put in active, retention, and deep sleep modes.

In this work, a high data retention 6T SRAM cell using a dual sleep transistor-based power gating technique is proposed for low-power IoT applications. The proposed architecture allows for independent control of both a PMOS header and an NMOS footer sleep transistor, thus providing three different operating modes: active mode, retention mode, and deep sleep

mode. The proposed architecture allows for fine control over leakage current by selectively gating both supply and ground rails. This leads to significant leakage suppression while maintaining sufficient voltage across internal storage nodes during retention mode. Unlike traditional techniques that employ only a single sleep transistor, this proposed work does not completely discharge the internal storage nodes, thus providing better data stability.

The novelty in this work is based on the integration of dual sleep transistor power gating with duty cycle aware energy analysis, thus facilitating the realistic analysis of energy consumption in SRAM memory devices based on IoT operation scenarios. Instead of using static leakage as a measure, this methodology has been developed to analyze total energy consumption in SRAM memory devices by taking into consideration mode-dependent leakage currents and their respective ratios. The proposed architecture has been validated through netlist-based LT Spice simulations in a CMOS technology node, with in-depth analysis of leakage current, storage node voltage retention, and supply current for all modes of operation. The proposed architecture has shown significant leakage current reduction in retention and deep sleep modes while ensuring data retention, thus validating its suitability for IoT devices.

2. Related Work

Recent studies in Static Random Access Memory (SRAM) have been focused on achieving an optimal balance in stability, performance, and power efficiency, particularly in low-power Internet of Things (IoT) applications, in which devices are operated with stringent power constraints. In [1], a low leakage and highly stable SRAM cell was developed to overcome the adverse effect of process variation, which becomes significant in deep submicron technologies. This study improves data retention stability and reliability for different operating conditions. Another study in [2] reported an ultra-low power consumption SRAM bit-cell using 45nm CMOS technology, in which optimal sizing and structural optimization were used to improve noise margins and access times for better performance. The study in [3] further focused on techniques to improve both read and write operations for better performance by regulating node voltages and minimizing unnecessary switching activities to minimize dynamic power consumption. In addition, [4] reported a comparative study of different low-power techniques for conventional 6T SRAM cells, in which power, delay, and area trade-offs were discussed in detail. The above studies demonstrate that, despite various advancements in

this area, achieving high stability with low power consumption and area is still a significant challenge in SRAM design.

Meanwhile, leakage power reduction is a significant focus area, especially in IoT systems where the memory is in a stand-by state for a considerable time. The sleep-stack technique introduced in [5] reduces sub-threshold leakage power by inserting more transistors in series, thus limiting the path of the leakage current. The application of power gating techniques at the circuit level in [6] disconnects the power supply when the memory is not in use, thus reducing the leakage power significantly and improving the battery life. The same idea was implemented in [7], where a sleep-based technique is introduced to reduce the energy consumption in the standby state of the 6T standard SRAM cell. Advanced techniques like the one presented in [8] combine power gating and dual gate MOS structures to reduce leakage power further. The foundational work in [9] introduced the dynamic sleep transistor technique, which paved the way for the development of the latest low power SRAM architectures, and [10] showed the possibility of sub-threshold operation in SRAMs, thus saving a significant amount of energy. However, upon closer inspection, it is found that most methods focus on leakage reduction or stability improvement individually and do not take into account real-time operating conditions such as duty cycles. In real-world IoT applications, memory activities are not constant, and duty cycles are neglected, resulting in inefficient energy usage. To address this problem, this work proposes a High-Data-Retention 6T SRAM cell that includes dual sleep transistor-based power gating and duty cycle-based energy analysis for better leakage reduction, data retention, and efficient energy usage.

3. Proposed Work

3.1 Conventional 6T SRAM Cell Overview

The conventional 6T SRAM cell architecture comprises two cross-coupled CMOS inverters realized with pull-up PMOS and pull-down NMOS transistors, and two access NMOS transistors connected to complementary bit-lines. This architecture provides bistable operation with reliable read and write operation during nominal operation. The conventional 6T SRAM architecture has been popular due to its simplicity and reliability in mainstream memory implementations.

Nevertheless, in scaled CMOS technologies, the conventional 6T SRAM architecture faces significant issues with large standby leakage current due to subthreshold conduction, gate tunneling, and junction leakage mechanisms. The leakage current in scaled CMOS technologies grows exponentially with decreasing feature sizes, causing significant power consumption in idle periods. This is particularly critical for IoT and edge computing applications, where SRAM blocks are in idle mode for long periods with occasional active operation. Hence, for low-power, energy-constrained applications, the conventional always-on 6T SRAM architecture is no longer suitable for applications with stringent leakage current requirements while ensuring data retention reliability.

3.2 Dual Sleep-Transistor Power-Gated SRAM Cell

In order to reduce standby leakage and retain stored information, the proposed SRAM architecture utilizes dual sleep transistor power gating techniques to the conventional 6T SRAM cell structure, as depicted in Fig. 1. To achieve this, a PMOS header sleep transistor is added between the SRAM cell and the supply voltage (VDD), and another NMOS footer sleep transistor is added between the SRAM cell and ground (VSS). The two sleep transistors can be independently controlled to allow for flexible and finer control of the SRAM operating modes.

The dual configuration of the sleep transistor, as depicted in Fig. 1, achieves improved leakage suppression with respect to traditional single sleep transistor schemes, owing to the simultaneous restriction of leakage paths on both the supply and ground sides. The dual-gating configuration significantly minimizes sub-threshold leakage current during low-power operation. On the other hand, partial power supply is enabled during the retention mode, ensuring the storage node voltage levels remain within the data-retentive range. The above configuration of the dual sleep transistor architecture, therefore, strikes an optimal balance between leakage suppression and data stability without the need for additional retention circuits or complex biasing schemes, making it suitable for ultra-low-power IoT memory design.

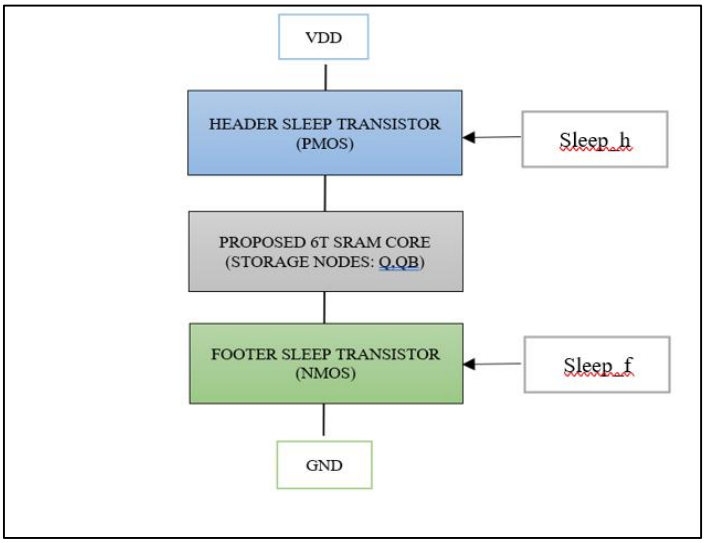

Figure 1. Proposed SRAM Architecture with Dual Sleep Transistor Power Gating

3.3 Operating Modes

Based on the dual sleep-transistor configuration shown in Fig. 1, the proposed SRAM cell supports three distinct operating modes tailored for duty-cycled IoT workloads:

- **Active Mode:** Both the header and footer sleep transistors are turned ON (Sleep_h = 1, Sleep_f = 1), providing full connectivity to VDD and VSS. In this mode, the SRAM cell operates normally and supports standard read and write operations with minimal performance impact.

- **Retention Mode:** The header sleep transistor remains ON while the footer sleep transistor is turned OFF (Sleep_h = 1, Sleep_f = 0). This configuration significantly reduces leakage current while maintaining sufficient internal node voltage to preserve stored data. Retention mode is suitable for moderate idle intervals requiring fast wake-up.

- **Deep Sleep Mode:** Both the header and footer sleep transistors are turned OFF (Sleep_h = 0, Sleep_f = 0), providing maximum leakage reduction. As shown in Fig. 1, this mode effectively isolates the SRAM cell from the power rails while allowing controlled leakage paths for partial data retention during extended idle periods.

3.4 Advantages of the Proposed Architecture

The proposed dual sleep transistor-based SRAM architecture provides several advantages, making it extremely appropriate for energy-constrained IoT devices. The most significant advantage is that the leakage current is minimized in stand-by, retention, and sleep modes. In addition, data retention is improved in comparison to traditional single transistor-based power-gating techniques, which are known to cause increased data instability. The use of header and footer sleep transistor-based independent control provides a fine-grained approach to power management, allowing for more flexible operation in different working scenarios. Finally, the proposed SRAM cell-based architecture requires minimal structural changes to the traditional 6T SRAM cell, thus reducing design complexity. In addition, the proposed design is highly compatible with traditional duty-cycled operation scenarios in IoT devices.

3.5 Implementation Considerations

The architecture as shown in Figure 1 has been fully transistor-level modeled using netlist-based LT Spice simulators without the need to construct the circuits at the schematic level. Such control allows the accurate assessment of the leakage currents as well as the data retention ability of the circuits when operating at various power modes. The header transistor, PMOS, as well as the footer transistor, NMOS, have been accurately sized in order to ensure the minimization of the leakage currents without compromising the ability of the circuits to maintain the voltages at the storage nodes. Such simplicity makes the proposed architecture compatible with the conventional 6T SRAM architectures. In addition, the simplicity of the proposed architectures makes the architectures suitable for the development of IoT-based systems.

4. Simulation Setup and Methodology

Using a recently proposed SRAM cell design, the data retention characteristics and the power consumption for various modes of operations at the architectural level are studied. The proposed SRAM cell is characterized and the impact of different architectural features on its data retention characteristics and power consumption is explored by netlist-level simulation in LT spice, obviating the need for the time-consuming task of circuit design from scratch. Since the proposed design at the schematic level is not required, it is possible to speed up the

investigation process of different operating modes of the SRAM cell by focusing on the architectural level of design. To focus on the leakage currents, all simulations are done by using Level-1 MOSFET models characterized for a 45 nm CMOS technology where the device dimensions are so small that sub-threshold leakage current and gate oxide leakage current are the main contributors to the total power consumption of SRAM cells.

The nominal supply voltage for the transistor operation was fixed at 1V which is representative of low voltage CMOS operation. The temperature was fixed at room temperature (T = 27 °C) in order to provide benchmark for further temperature dependent leakage investigations. The steady state electrical behavior of the SRAM cell was obtained via DC operating point (.op) analysis. This provided a clear illustration of the node voltages, the leakage currents, and the static internal stability of the cell under its different modes of operation which are; Active, Retention, and Deep Sleep. Hence it gives clear insight into leakage dominated power consumption, which can then be compared to that of a typical SRAM where the effectiveness of the low power characteristics of the SRAM design can be ascertained.

4.1 Sleep Control Configuration

Two independent sleep control signals were incorporated in the netlist to enable fine-grained power gating:

- Sleep_f: Footer NMOS sleep control (virtual ground gating)
- Sleep_h: Header PMOS sleep control (virtual supply gating)

Using these controls, three operating modes were realized:

1. Active Mode: Sleep_f = 1, Sleep_h = 1
2. Retention Mode: Sleep_f = 1, Sleep_h = 0
3. Deep Sleep Mode: Sleep_f = 0, Sleep_h = 0

This configuration allows selective disconnection of the supply and ground paths while ensuring data preservation during retention mode and maximum leakage suppression during deep sleep.

4.2 Measured Parameters

For each operating mode, key parameters were extracted directly from DC operating point analysis:

1. Supply current, I(VDD), used to quantify static leakage power
2. Storage node voltages, V(Q) and V(QB), to verify data stability and retention
3. Virtual supply and ground node behavior, to assess the effectiveness of dual sleep-transistor power gating

All measurements were obtained exclusively through netlist-based probing, ensuring repeatability and eliminating schematic-dependent variations.

4.3 Sleep Transistor Width Sweep

For evaluating the design tunability of the proposed design, a parametric sweep (.step) analysis is performed on the width of the sleep transistor. During this analysis, all other circuit parameters remain constant. The parametric sweep analysis evaluates the influence of the sleep transistor on the reduction of leakage current and the stability of the storage node voltage during retention and deep sleep modes. By varying the width of the sleep transistor, the sensitivity of the standby leakage and virtual supply degradation can be evaluated. The analysis can also be used to determine the point of diminishing returns beyond which increasing the width of the sleep transistor does not show any significant improvement in leakage reduction and voltage stability. The analysis can help in evaluating the trade-off between leakage reduction and area overhead in nanoscale SRAM designs. The analysis can help in choosing the optimal width of the sleep transistor for IoT applications.

4.4 Duty-Cycle Aware Energy Estimation

To evaluate the energy efficiency of the proposed SRAM cell under realistic IoT operating conditions, a duty-cycle aware energy model is employed. The memory operation is divided into three modes: active, retention, and deep sleep, each occupying a fraction of the total operating period.

The average supply current over one operation cycle is computed as

$$I_{\text{avg}} = D_A I_A + D_R I_R + D_D I_D \quad (1)$$

where I_A, I_R, and $I_D$are the supply currents in the active, retention, and deep sleep modes, respectively, and D_A, D_R, and $D_D$are the corresponding duty-cycle fractions, satisfying $D_A + D_R + D_D = 1$. Thus, the average current is obtained as the duty-cycle weighted sum of mode currents (1).

The total energy consumption per operation cycle is given by

$$E_{\text{total}} = V_{DD}\, I_{\text{avg}}\, T_{\text{cycle}} \tag{2}$$

where $V_{DD}$is the supply voltage and $T_{\text{cycle}}$is the cycle duration. Equation (2) allows direct comparison of energy consumption across different sleep configurations and transistor sizing options.

5. Results and Discussion

This section includes the simulation results for the proposed dual sleep transistor-based 6T SRAM cell and assesses its effectiveness in reducing leakage, retaining data, and achieving duty cycle-aware energy efficiency, especially for IoT-based applications where energy constraints are critical. The effectiveness of the proposed SRAM cell is also compared in different operating modes.

5.1 DC Operating Point Analysis

In order to validate the stability and leakage characteristics of the suggested SRAM cell, DC operation point simulations (.op) were carried out in LT Spice under different modes of operation, as dictated by the sleep signals. The steady-state voltage levels at the storage nodes, V(Q) and V(QB), were monitored to validate the proper data retention capability under all modes of operation, including active, retain, and deep sleep modes. At the same time, the supply current, I(VDD), was also monitored to measure the static current under each mode. The effects of activating the header and footer sleep transistors were monitored. Once the sleep transistors are activated, the virtual supply voltage, VDD_virtual, and virtual ground, GND_virtual, nodes disconnect the SRAM cell from the main supply rails, thus suppressing the leakage current without affecting the data.

From the simulation results presented in Table 1, it is evident that the proposed design maintains the storage node voltages and reduces the leakage currents to a great extent during

retention and deep sleep modes. The dual sleep transistor-based design is thus validated as providing improved data retention and low-power operation to the proposed SRAM cell.

Table 1. DC Operating Point of Proposed 6th SRAM Cell with Dual Sleep-Transistor Power Gating

Mode	Vsleep_f	Vsleep_h	V(q) [V]	V(qb) [V]	I(VDD) [A]
Active	1	1	0.450039	0.450039	-1.68487×10^{-12}
Retention	1	0	0.440294	0.440294	-3.22412×10^{-12}
Deep Sleep	0	0	0.303425	0.303425	-1.65244×10^{-12}

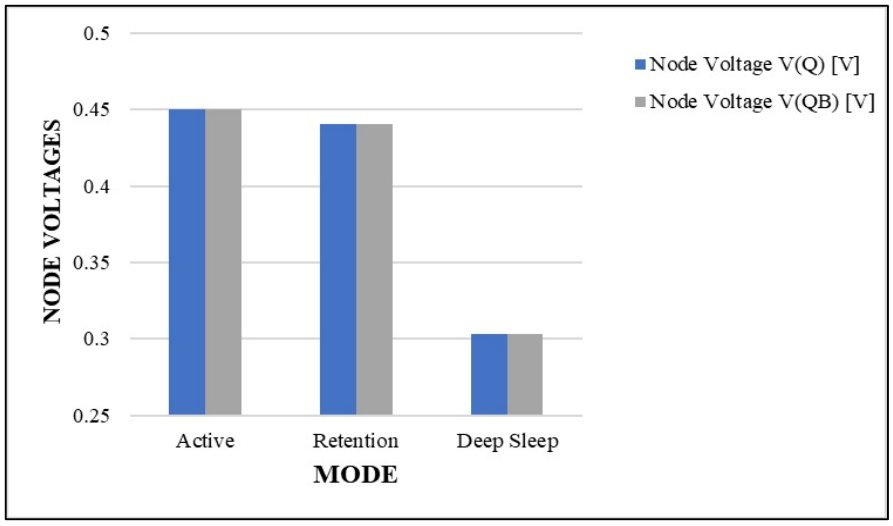

Figure 2. Storage Node Voltages V(Q) and V(QB) Across Different Operating Modes, Demonstrating Stable Data Retention

Figure 2 shows the variation of storage node voltages V(Q) and V(QB) across the three operating modes of the proposed SRAM cell, thereby validating the data retention capability of the SRAM cell. In active mode, both the sleep transistors are enabled, thereby providing full supply connections. In retention mode, as illustrated in Figure 2, there is a reduction in leakage current, but the voltage levels of the nodes Q and QB are sufficient to retain the data, as indicated by the marginal reduction in voltage levels. In deep sleep mode, the voltage levels of the nodes Q and QB decay more, but the voltage levels are sufficient during the long idle intervals of IoT devices, thereby validating the effectiveness of the proposed SRAM cell.

5.2 Mode-Wise Leakage Current Comparison

To explicitly compare leakage behavior across modes, the measured supply current values are summarized in Table 2.

Table 2. Mode-Wise Leakage Current Comparison

Mode	I(VDD) [A]
Active	-1.68487×10^{-12}
Retention	-3.22412×10^{-12}
Deep Sleep	-1.65244×10^{-12}

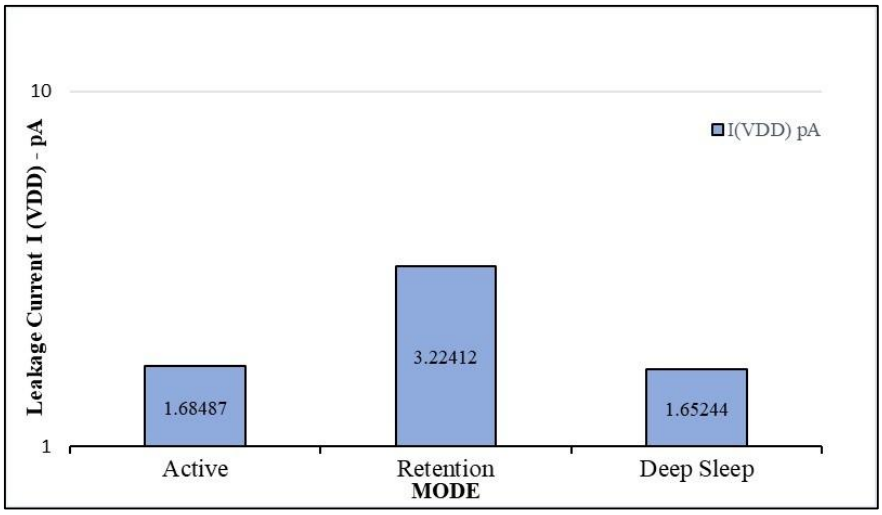

Figure 3. Mode-Wise Leakage Current Comparison of the Proposed SRAM Cell Under Active, Retention, and Deep Sleep Modes

Fig. 3 presents the mode-wise leakage current comparison of the proposed SRAM cell across active, retention, and deep sleep operating modes. As observed in Fig. 3, the leakage current in retention and deep sleep modes is significantly reduced compared to active operation, validating the effectiveness of the dual sleep-transistor power-gating strategy.

5.3 Sleep Transistor Width Sweep Analysis

To evaluate the impact of sleep transistor sizing on data stability and leakage, a parametric width sweep was performed in sleep mode. The results are shown in Table 3.

Table 3. Sleep Transistor Width Sweep Results

Wsleep (µm)	V(q) [V]	I(VDD) [A]
0.2	0.400219	−3.826 pA
0.5	0.400219	−3.826 pA
1.0	0.400219	−3.826 pA

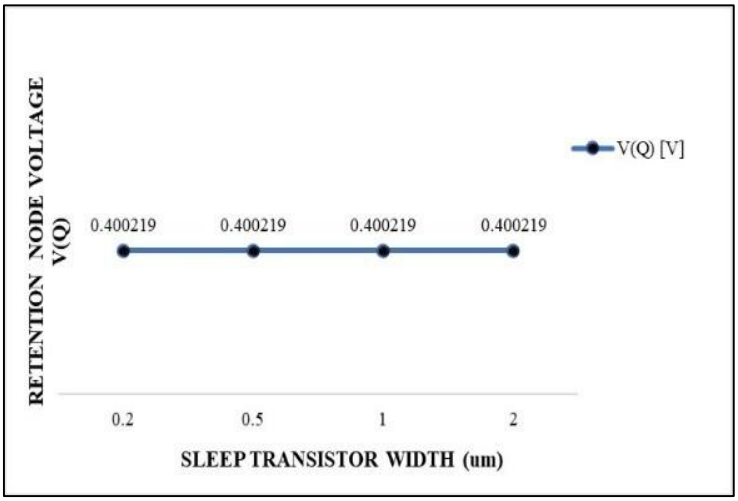

Figure 4. Effect of Sleep Transistor Width on Retention Node Voltage V(Q), Showing Robustness Against Sizing Variations

From the results in Fig. 4, it is evident that after a certain minimum width, the increase in the sizing of the sleep transistor does not have a significant impact on the retention voltage and leakage current. Thus, the effectiveness of the suggested architecture is validated in terms of its robustness in handling the sizing issue and enabling the designer to optimize the silicon area without affecting the leakage suppression and stability of the data. Such an aspect is advantageous in the implementation of the scalable SRAM array architecture in IoT systems.

5.4 Duty-Cycle Aware Energy Estimation

To simulate realistic workloads for IoT applications, duty cycle-aware energy analysis was carried out using post-processed leakage currents obtained from LT Spice simulation results. The total energy contribution for each operating mode was calculated by multiplying the supply current value with its respective activity ratio over a duty cycle. This simulates realistic workloads for IoT applications, where idle times are significant. Mode-wise energy contributions are realistic estimates of memory energy and are provided in Table 4.

Table 4. Duty-Cycle Aware Energy Estimation

Mode	I(VDD) [A]	Duty Cycle (%)	Energy Contribution [J]
Active	1.68487×10^{-12}	5	8.42×10^{-14}
Retention	3.22412×10^{-12}	15	4.84×10^{-13}
Deep Sleep	1.65244×10^{-12}	80	1.32×10^{-12}

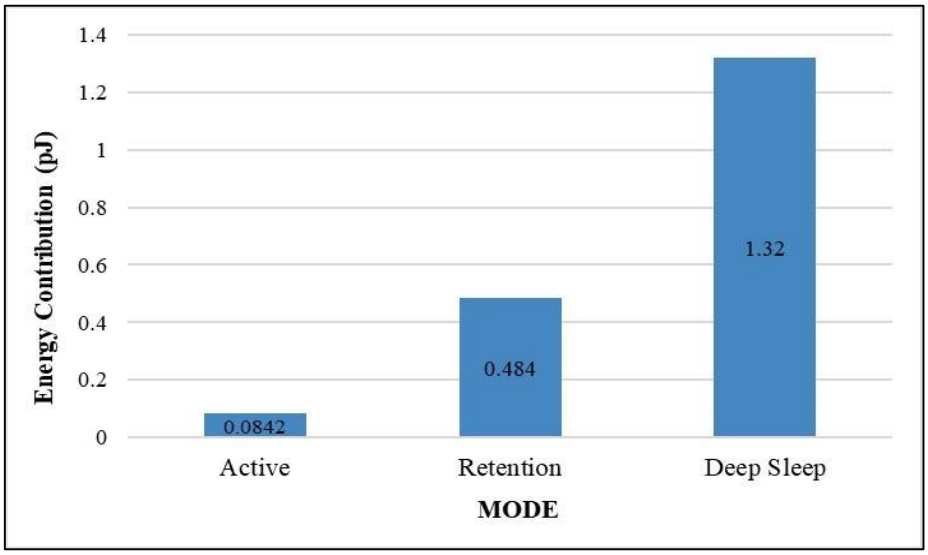

Figure 5. Duty-Cycle-Aware Energy Contribution of the Proposed SRAM Cell Across Active, Retention, And Deep Sleep Modes Under a Representative IoT Workload

Figure 5 illustrates the duty cycle-aware energy contribution of the proposed dual sleep transistor-based 6T SRAM cell for a representative IoT workload. Although the active mode contributes only 5% to the total duty cycle, its energy contribution remains low because of the ultra-low leakage current characteristic of the scaled 45nm transistors. The retention mode, contributing 15% to the total duty cycle, contributes moderate energy while ensuring data retention. The deep sleep mode contributes significantly to the total duty cycle at 80%, and its leakage current is lowest among all three modes, thus saving significant energy in the long run. These results cumulatively prove that the proposed SRAM architecture is efficient in reducing total energy while ensuring data retention integrity, thus making it more suitable for IoT applications where duty cycle is high and energy efficiency is critical.

6. Conclusion

This work has presented a high data retention 6T SRAM cell based on dual sleep transistor power gating for low-power applications in IoT devices. Independent control of header PMOS and footer NMOS sleep transistors enable three different modes of operation: active, retention, and deep sleep. Netlist-based LT spice simulations for a 45 nm CMOS technology and a 1V supply voltage have shown stable storage node voltages and significant leakage savings in retention and deep sleep modes compared to active mode. In addition, a width sweep for sleep transistor width has shown that the design is tunable to optimize leakage savings and robustness. Finally, duty cycle aware energy estimation has shown significant energy savings for realistic IoT workloads. In summary, a scalable and energy-efficient SRAM architecture is presented for ultra-low-power applications in IoT devices. It is worth mentioning that further enhancements can be achieved by applying array integration and sophisticated power management techniques.

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