

Emerging Nanoelectronic Technologies for Next-Generation VLSI: Devices, Challenges, and Prospects

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Abstract

The continuous scaling of CMOS technology enables significant progress in performance and integration density in VLSI. However, due to short-channel effects, leakage currents, interconnection delays, variability effects, and power-density limitations, at the current sub-5 nm feature size, the conventional scaling down of CMOS is becoming more and more challenging. This research work discusses a few promising nanoelectronic devices beyond the conventional CMOS, such as CNTFETs, TFETs, nanowire FETs, SETs, graphene-based devices, and spintronic devices. The principle of operation, characteristics, scalability, CMOS compatibility, and perspectives of VLSI application of the devices under consideration are comparatively analyzed. Possible problems related to the integration of the devices, including fabrication scalability, device variability, process complexity, cost, reliability, and thermal issues, are discussed. It is shown that heterogeneous and monolithic 3D integration can be effective methods for combining special-purpose nanoelectronic devices with traditional CMOS technology. Perspectives related to the application of 2D materials and negative-capacitance devices are discussed.

Keywords: VLSI, Nanoelectronics, Beyond-CMOS, CNTFET, TFET, Nanowire FET, Single-Electron Transistor, Graphene, Spintronics, Nanotechnology.

1. Introduction

For more than fifty years, the semiconductor industry has adhered to Moore's Law, which described that the transistor count on integrated circuits approximately doubles every two

years [1]. This scaling led to continuous doubling of performance, power efficiency, and cost, effectiveness of Very Large-Scale Integration (VLSI) systems among many other advantages. The main CMOS technology has been continuously improved with every new technology node in terms of speed and integration density. However, as transistor dimensions shrink further to the sub 5 nm range, the limitations of silicon-based CMOS technology become very clear [2].

Several quantum mechanical effects such as direct source to drain tunnelling, leakage of gate dielectric, and random variations in dopant concentration make device behaviour unpredictable. Moreover, the power density has increased to such an extent that it is very difficult to keep the chip cool using traditional methods. With resistivity and capacitance of interconnects also contributing more to circuit delay, the advantages of transistor scaling are declining. Overall, these issues indicate that relying solely on CMOS scaling will no longer provide the performance improvements achieved in previous technology generations [3]. Following documents such as the International Roadmap for Devices and Systems (IRDS) [4], the global semiconductor industry has recognized several beyond-CMOS device technologies that could either complement or substitute conventional transistors. They cover devices based on carbon nanomaterials, quantum tunnelling, single electron phenomena, two dimensional (2D) materials, and spin polarized transport. All of the methods are based on using different physical effects which might provide benefits in terms of energy efficiency, switching speed or size.

This paper provides a comprehensive review of the latest nanoelectronic device technologies. It also evaluates these devices from the perspective of VLSI integration. Section 2 points out the limitations of the conventional CMOS when scaled down to nanoscale. Section 3 introduces the working principles and features of six main beyond-CMOS device families. Section 4 gives an overview of VLSI integration possibilities. Section 5 highlights the major challenges. Section 6 offers future perspectives and roadmap alignment while Section 7 concludes the review.

2. Limitations of Conventional CMOS at Nanoscale

The impressive advancements made possible by the technology of complementary metal oxide semiconductor (CMOS) can be attributed to the continual scaling of transistors, resulting in high levels of integration, better performance, and reduced cost per function. As the technology of CMOS transistors continues to scale to below 5 nm, the scaling is hindered by certain physical

and technological limits that greatly inhibit any improvement in terms of performance, energy efficiency, and reliability. Some of these limits include quantum, electrostatic, power, process, and interconnect limits [5].

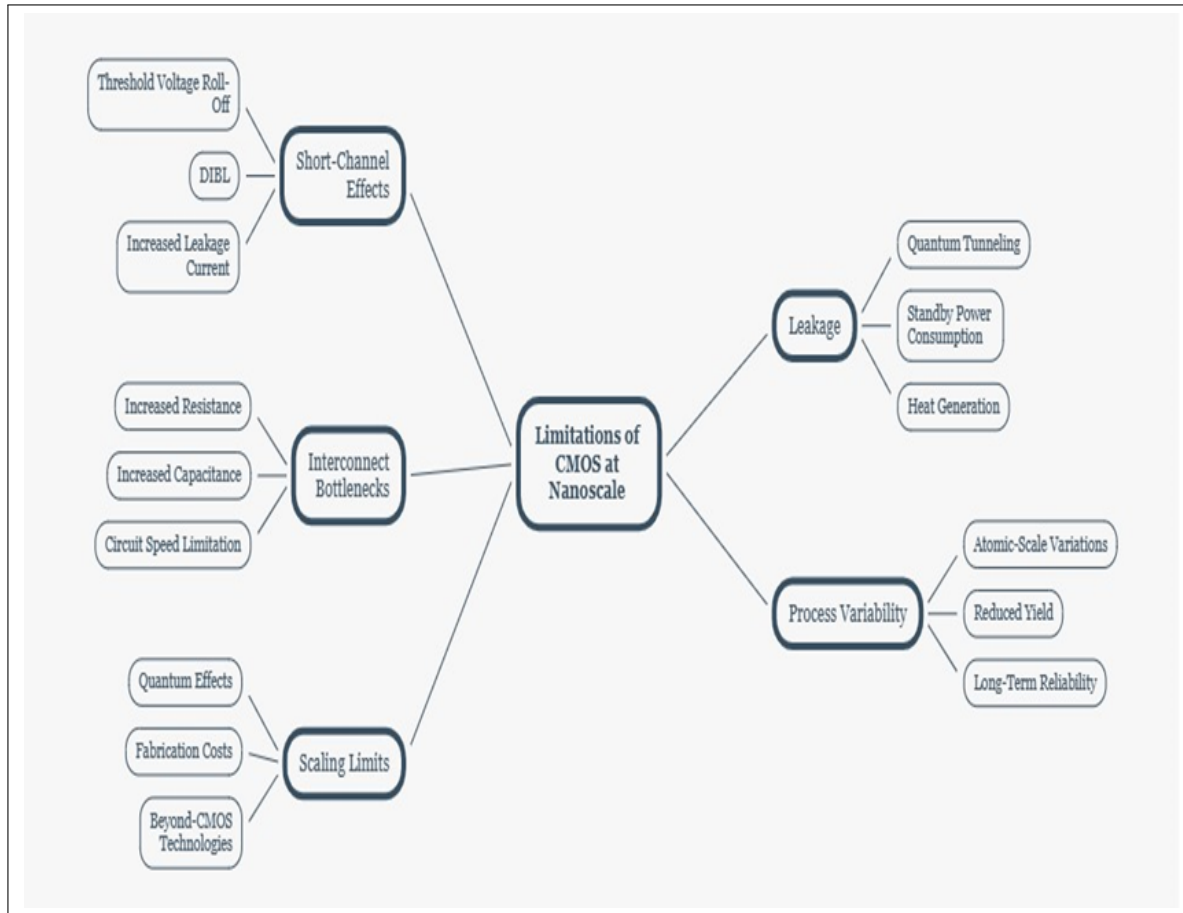


Figure 1. Major limitations of conventional CMOS technology at the nanoscale.

2.1 Short-Channel Effects

With the reduction of the channel length to the nanometer scale of the MOSFET, the gate's ability to exercise electrostatic control over the channel is lost due to the increased effect of the electric fields generated at the source and drain sides. This leads to short-channel effects (SCEs) like threshold voltage roll-off, drain-induced barrier lowering (DIBL), higher off-state leakage current, and subthreshold swing deterioration [2]. These issues not only affect the performance of the devices but also limit their future scaling down.

New generations of transistors such as FinFETs and gate-all-around (GAA) nanowire transistors have been developed to overcome the issue of reduced electrostatic control through multi-gate structure. While these transistors do provide significant suppression of the SCEs, they

are complicated to manufacture and cannot overcome the physical limitations of scaling [5].

2.2 Leakage Currents and Power Dissipation

Power dissipation has emerged as one of the most serious problems in nanometer CMOS devices. Dynamic power consumption is directly related to the frequency of switching operations, load capacitance, and the square of the supply voltage, while static power consumption is mainly due to subthreshold leakage current and gate oxide tunneling currents. With the reduction of the device size to less than 10 nm, quantum tunneling through the gate oxide films and band-to-band tunneling are the main sources of leakage, hence leading to large increments in standby power consumption [6].

Furthermore, due to further miniaturization, operational voltage is not scaled down proportionally; hence, power density is increased significantly. Heat generation causes reliability and lifetime problems for the device. CMOS switching is at the thermodynamic limits of binary logic, which makes future improvement very difficult.

2.3 Interconnect Bottlenecks

With the ongoing process of miniaturizing devices, interconnect delay is becoming one of the crucial constraints on performance of the circuit. With the decrease in the dimensions of the copper interconnects, the electron scattering due to surfaces and grain boundaries results in increasing resistance, whereas the capacitance effect between neighboring metallic interconnects still remains important. Hence, RC delay of interconnects often becomes higher than the transistor switching delay in advanced technological nodes [7].

Not only does high resistance slow down the operation of the circuit, but it also causes power dissipation and poses reliability problems in terms of electromigration. Therefore, various alternative materials for interconnects, such as carbon nanotubes and graphene, are being considered because of their high conductivity and ability to carry high currents due to better thermal properties of these materials.

2.4 Process Variability and Reliability

As the size of the transistors becomes smaller at the atomic level, variations in the manufacturing process will greatly affect the properties of the devices. Variations in the threshold voltage, drive current, and leakage properties can be caused by variations in random

dopant distribution, line-edge roughness, gate length variation, and oxide thickness fluctuation. Such variations lead to decreased device yield and difficulties in time closure in large-scale integrated circuits [5].

Reliability problems like bias temperature instability (BTI), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and electromigration also become serious in advanced CMOS technology.

2.5 Fundamental Scaling Limits

The continuation of Moore's Law becomes more and more limited by several physical and economic constraints. Since the dimensions of transistors come close to several atomic layers, quantum confinement, direct tunneling between source and drain contacts, and impossibility to lower supply voltage any more restrict the possibility of performance and energy efficiency improvement. On the other hand, the rising costs of advanced lithographic equipment and facilities make further CMOS scaling not economically viable. In this connection, there appears a considerable interest in developing the beyond-CMOS technologies such as carbon nanotubes field effect transistors (CNTFET), tunnel field effect transistors (TFET), nanowire transistors, graphene transistors, spintronic devices, and so on. These novel technologies intend to go beyond conventional CMOS while offering improved energy efficiency, switching behavior, and computational capabilities for future VLSI systems [4], [7].

3. Emerging Nanoelectronic Devices

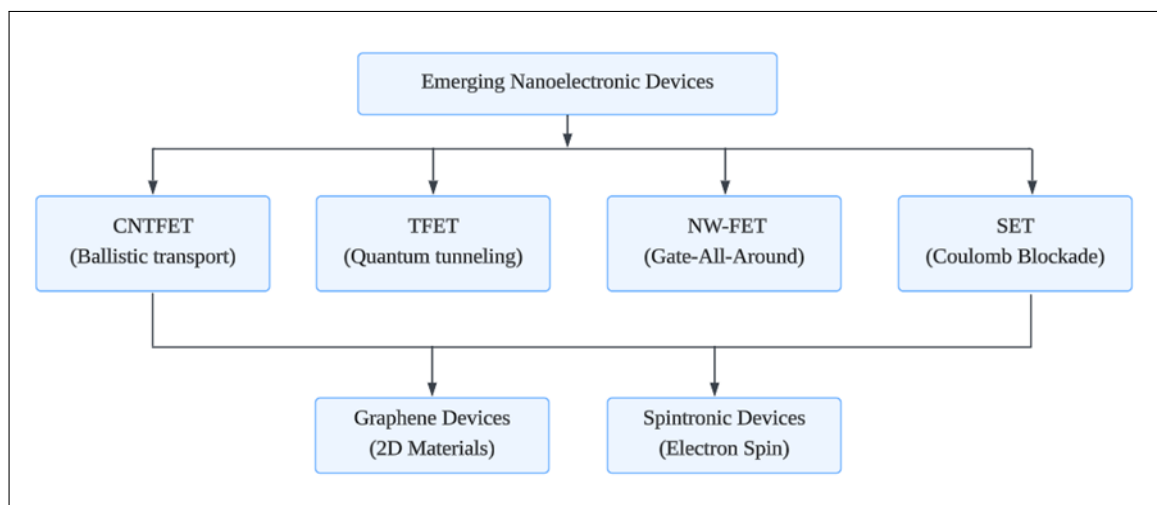


Figure 2. Emerging nanoelectronic devices

The physical constraints of nanoscale CMOS electronics have driven intensive studies in developing alternate device structures that can support progress in computing capability, energy consumption, and circuit scaling. Known generally as beyond-CMOS devices, the nanoelectronics devices use new concepts of charge transport, quantum effects, low-dimensional materials, and electron spin to circumvent the physical restrictions imposed by the conventional silicon MOSFET devices. Although no single concept is available to replace the CMOS device as a universal choice, there have been some promising ideas that can be explored for future VLSI systems.

3.1 Carbon Nanotube Field-Effect Transistors (CNTFETs)

The carbon nanotube field effect transistors (CNTFET) use semiconducting single-walled carbon nanotubes (SWCNTs) as the channel material, rather than silicon. Due to their 1D structure, carbon nanotubes have very fast and close to ballistic transport, very high carrier mobility, high thermal conductivity, and high current carrying capacity. This allows CNTFETs to operate at higher frequencies, lower supply voltages and lower power consumption as compared to silicon MOSFETs [3], [8].

One more major benefit of the CNTFET is that due to its strong electrostatic gating, the short-channel effects are suppressed, and it allows for aggressive device scaling. Besides that, CNT transistors show better energy delay properties that make them promising for high performance and low power computing applications.

However, there are some obstacles on the way to the implementation of large-scale commercialization of CNTFETs, such as chirality control, metallic nanotube separation, wafer scale alignment, reproducibility and compatibility with CMOS technology. As a result, CNTFET still remains an area of intensive research for future logic and interconnect applications.

3.2 Tunnel Field-Effect Transistors (TFETs)

Band-to-band quantum tunneling is used in Tunnel field effect transistors (TFETs) to replace thermionic emission in carrier injection. In contrast to regular MOSFETs, it is theoretically possible to get a subthreshold swing less than the thermal limit of 60 mV/decade in TFETs that would allow lower voltage operation with less power consumption [10].

Since the switching mechanism of the device relies on quantum tunneling, TFETs are

well-suited for use in low-power applications like wearable technology, bio-medical devices, wireless sensor networks, and IoT devices. Different material systems, like silicon, SiGe, and III–V semiconductor heterostructures, have been considered to enhance the efficiency of tunneling and boost the ON-state current.

On the other hand, there are some constraints in TFETs, which include relatively low ON current, susceptibility to interface traps, trap-assisted tunneling, and difficulty in fabricating because of the heterojunction structure [11].

3.3 Nanowire Field-Effect Transistors (NW-FETs)

The nanowire FETs or NW-FETs use nanowires of semiconducting materials as conduction channels and usually operate on the principle of the gate-all-around structure, wherein the gate surrounds the channel in all dimensions. Due to their superior electrostatics, these transistors exhibit very low short-channel and leakage current effects when compared to planar MOSFETs [12].

Several materials including silicon, germanium, and III–V compound semiconductor nanowires have been used for designing high performance transistors. Junctionless nanowire transistors simplify the fabrication process even further by using the simple gate structure without the formation of any abrupt source-channel-drain junctions.

The GAA nanowire transistors are seen as the natural evolutionary successor of FinFET technology, and are already being used in advanced semiconductor technology roadmaps. Thus, NW-FETs are one of the most mature beyond-CMOS technologies at present.

3.4 Single-Electron Transistors (SETs)

SETs utilize the Coulomb blockade effect that allows for the transportation of a single electron within a nanometer-scale island, thus providing for switching with an extremely low amount of energy spent on the process. The functioning of a SET is based on the principle when the energy needed for the charge is higher than the thermal energy of the electrons, thus making it possible to control the process of transportation of electrons due to quantum tunnelling [13].

Due to the fact that only one electron is involved in the switching, SETs provide for a very low amount of energy used and can approach the theoretical minimum switching energy according to Landauer's principle. This makes SETs interesting in the field of ultra-low-power

electronics, quantum information processing, and also charge measurement devices.

Despite the fact that the practical use of such devices may be problematic since the operation at room temperature is only feasible with nanometer-scale islands, less than 10 nm in size.

3.5 Graphene-based Devices

Graphene is a one-atom thick material made up of a honeycomb network of carbon atoms. It has exceptional properties related to electron conduction and thermal and mechanical conductivity [8].

The graphene field effect transistors (GFETs) demonstrate very high carrier transport velocities and good high-frequency behavior. They are especially attractive for radio frequency (RF), analog, flexible and high-speed communication applications. In addition, graphene holds promise for transparent electronics and wearable devices.

However, the absence of the intrinsic gap in graphene leads to low ON/OFF ratio that makes the material less attractive for logic applications. Many methods, such as nanoribbons of graphene, bilayer graphene, strain engineering, and chemical modification of graphene, were tried to obtain the gap in the graphene material.

3.6 Spintronic Devices

In addition to the inherent electrical charge of electrons, spintronic devices make use of their spin state to perform operations related to storing and processing of information. Since spintronic devices are designed using spin polarization, instead of simply relying on charge transport, these devices exhibit a number of desirable properties such as non-volatility, low energy consumption for switching, high durability, and good resistance to radiation [15].

Magnetic tunnel junctions (MTJs) constitute the basic unit of numerous spintronic devices, especially the spin-transfer torque magnetic random-access memory (STT-MRAM) that is already commercially available for embedded memory applications. Combining the use of STT-MRAM with the latest CMOS technologies results in high-performance, non-volatile memory with reduced power dissipation.

Despite the commercial success of spintronic memory technologies, spin-based logic devices that can replace the traditional CMOS transistor have not been able to compete on account of switching speed, gain, and room temperature performance. Hence, at present,

spintronics is considered a complementary technology to CMOS technology.

3.7 Comparative Assessment of Emerging Nanoelectronic Devices

The main strengths of each beyond-CMOS technology lie in overcoming the weaknesses of conventional silicon transistors. Thus, CNTFETs have extremely high carrier mobility and speed, TFETs operate at ultra-low voltage levels, NW-FETs are scalable and compatible with CMOS technology, SETs consume extremely low energy when switching, graphene-based structures show high promise in RF and flexible electronic applications, and spintronic devices can serve as nonvolatile memory that consumes low power in standby mode.

However, many issues still persist, such as manufacturability on a large scale, process variability, material compatibility, cost of manufacturing, reliability, and compatibility with existing semiconductor fabrication technologies. Consequently, the future of VLSI technology will be dominated by heterogeneous integration that combines CMOS technology with other specialized nanoelectronics.

4. VLSI Integration Prospects

4.1 Process Compatibility

A key factor in whether VLSI integration can be done at all is the degree to which it can make use of the same manufacturing infrastructure currently employed in semiconductor production. Among all the devices considered, GAA nanowire FETs, especially silicon ones present the best chances of being integrated since they are basically the next step in the evolution of FinFETs and have already been included in production schedules [4]. In a similar vein, TFETs using silicon or SiGe enjoy the advantage of going through CMOS compatible processes while on the other hand III, V and CNT based approaches need a substantial development of wafer scale integration.

4.2 Performance Benchmarking

Franklin [8] makes a comparative study of nanomaterial transistor performance versus traditional CMOS transistor performance. It is shown (through computations and simulations) that (carbon nanotube field effect transistors) CNTFETs and graphene RF transistors (radio frequency transistors) perform better than silicon in some performance parameters. Table 1 provides a summary of the main device characters which have been compared for different technologies.

Table 1. Comparative summary of beyond-CMOS nanoelectronic devices [4], [8]

Device	Supply Voltage	Switching Speed	Power Dissipation	Scalability	CMOS Compat.	Maturity
CMOS	~1.0 V	High	High	Limited	N/A	Mature
CNTFET	0.4–0.9 V	Very high	Very low	High	Moderate	Research
TFET	0.2–0.5 V	Moderate	Ultra-low	High	High	Research
Nanowire FET	0.5–0.8 V	High	Low	Very high	High	Research
SET	< 0.1 V	Low	Ultra-low	High	Low	Lab stage
Graphene FET	0.3–1.0 V	Extremely high	Low	High	Moderate	Research
Spintronic	~0.7 V	Moderate	Very low	Moderate	Low	Early stage

4.3 Application Domains

Different nanoelectronic devices are suited to different VLSI application domains. For instance, CNTFETs and graphene devices are highly competitive in the segment of high-speed analogue/RF circuits and interconnect applications. On the other hand, TFETs and SETs are considered to be the best candidates for super low power sensing and IoT edge devices. Besides, digital logic of very high density is the domain most suited to NWFETs. Lastly, among the spintronic MTJs they are the most developed type of embedded non-volatile memory. While examining the architectural consequences of beyond-CMOS devices pointed out that heterogeneous integration which is the mixing of different device types to different functional blocks could bring more practical near-term gains than a complete replacement of CMOS [7].

5. Challenges

5.1 Fabrication and Scalability

The main challenge for most beyond-CMOS technologies is the controlled synthesis, placement, and doping of nanoscale structures at the level of a wafer [8]. A single tube can neither be semiconducting nor metallic, as the synthesis of CNTs results in a mix of semiconducting and metallic tubes, which need to be separated with very high purity for logic applications. Positional control of nanowires is very limited when they are grown by vapor, liquid, solid (VLS)

mechanisms. Fabrication of single electron transistors with atomic precision is incompatible with the use of high throughput lithography. In some cases, directed self-assembly, atomic layer deposition, and scanning probe lithography have progressed, but they still fall short of the throughput needed for VLSI manufacturing.

5.2 Device Variability and Reliability

Variations in characteristics of devices due to atomic scale tolerances in the manufacturing process are very challenging to circuit design. CMOS has for a long time benefited from process improvements that have brought intra-die and inter-die variability down to levels that are manageable [5]. On the other hand, nanoelectronic devices are inherently more variable because their properties depend greatly on the specific atomic configurations. For instance, TFETs are extremely vulnerable to trap assisted tunnelling through interface states, which not only degrades their subthreshold slope but also results in increased variability [11]. Hence, it will be necessary to come up with circuit design methods that are able to handle high levels of device variability.

5.3 Integration Complexity and Cost

In the end, the economic feasibility of beyond-CMOS technologies must prevail the huge manufacturing capacity and learning curve benefits that silicon CMOS has. Introducing new materials and device architectures means a need for specialized deposition, etching, and characterization equipment. Combining materials from completely different systems in the process like III, V channels on silicon substrates, CNT networks on oxide dielectrics, leads to thermal budget limitations and contamination risks [7]. Economically viable solutions might be monolithic 3D integration, where nanoelectronic devices are fabricated in the back, end layers above the conventional CMOS, instead of replacing the basic silicon process.

5.4 Thermal Management

High performance operation of nanoelectronic devices in dense VLSI environments leads to a significant amount of heat being generated locally. Some devices like TFETs, for instance produce a lot less power per switch. However, their very use in high density arrays could still cause thermal issues. CNTs have unusually high intrinsic thermal conductivity along the tube axis but they are poorly thermally coupled to the surrounding dielectrics, thus limiting

the heat dissipation that is actually possible [3]. The evolution of thermal design along with device and architecture development will be necessary to make sure that the operation remains reliable. The major challenges associated with nanoelectronic device development, with their impacts and potential solutions are summarized in Table 2.

Table 2. Key challenges in nanoelectronic devices

Challenge	Key Issue	Impact	Potential Solution	Ref.
Fabrication & Scalability	Difficulty in CNT purification, nanowire placement, and atomic-scale fabrication	Limited wafer-scale manufacturing and low production throughput	Directed self-assembly, atomic layer deposition (ALD), advanced lithography	[8]
Device Variability & Reliability	Atomic-scale process variations and interface defects	Threshold voltage variation, reduced reliability, lower yield	Variability-aware circuit design and improved fabrication control	[5], [11]
Integration Complexity & Cost	Integration of new materials with CMOS requires specialized processes	Higher fabrication cost, contamination risk, thermal budget limitations	Monolithic 3D integration and heterogeneous integration	[7]
Thermal Management	High heat density and limited heat dissipation	Reduced performance and device reliability	Thermal-aware design, improved cooling techniques, high-conductivity materials	[3]

6. Future Roadmap and Prospects

6.1 Hybrid CMOS-Nanoelectronic Architectures

The best achievable and most realistic way to use nanoelectronic devices in VLSI very soon is through heterogeneous integration instead of total replacement of CMOS [7]. Hybrid architectures that use CMOS for the main logic and memory and while incorporating nanoelectronic devices for specialized functions like ultra-low-power sensing, high frequency RF, or non-volatile storage can provide system-level benefits and the way of reducing integration

risk. 3D monolithic integration where multiple device layers are vertically stacked with dense inter layer connections, is a manufacturing framework for such heterogeneous systems.

6.2 Alignment with IRDS Roadmap

The International Roadmap for Devices and Systems (IRDS) [4] explicitly names a few types of beyond-CMOS device families such as TFETs, nanowire FETs, and 2D material FETs as the main intended candidates for research investment. According to the IRDS, hybrid CMOS, nanoelectronic systems may become commercially viable during the 2028-2035 time period for certain application areas, and their mass-market adoption will depend on the success of the fabrication and variability issues discussed in Section 5.

6.3 Emerging Research Directions

Several research directions are emerging beyond the devices presented in this study. Transition metal dichalcogenides (TMDs) like MoS_2 and WSe_2 are examples of two-dimensional channel materials with bandgaps at the atomic level (i.e. the channel is only a few atoms thick). They have high electron mobility which is an attractive property of graphene but also have good on/off ratios that are suitable for digital logic [8]. Ferroelectric gate dielectric based negative capacitance FETs hold the potential to bust the 60 mV/decade Boltzmann limit in the CMOS device framework. Topological insulator surface states and Majorana fermion-based quantum computing are far ahead in the future and still undergoing a lot of speculations, but they can bring about radical changes.

7. Conclusion

This article has discussed some potential nanoelectronic technologies that can overcome the physical and technical constraints imposed by the nanoscale CMOS devices. CNTFET has very high carrier mobility and switching characteristics, while TFET can provide ultra-low power consumption characteristics. The GAA nanowire FET has shown excellent electrostatic performance and compatibility with CMOS devices. In addition, the SET devices have extremely low switching power consumption, whereas the graphene devices are useful at high frequencies and spintronic devices are nonvolatile. Still, at present, none of the devices possesses the combination of high performance, low power consumption, fabrication scalability, reliability, and CMOS compatibility, required to replace the conventional CMOS devices for VLSI applications.

The GAA nanowire FET and TFET can be integrated in the near future, while the CNTFET and graphene devices need fabrication advancements. Hence, the VLSI systems of the future can employ the heterogeneous approach with the integration of CMOS with specialized nanodevices.

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