

ENERGY AND POWER EFFICIENT SYSTEM ON CHIP WITH NANOSHEET FET

Dr. N. Mohan Kumar,
Professor,
Department of Electronics and Communication Engineering,
GITAM School of Technology, Bengaluru campus, India.
Email: mohankumar.nagarajan@gitam.edu

Abstract: As the level of integration of IC increases, System on Chip (SoC) design has evolved. This technology comprises of several intellectual property blocks on a single chip. With downsizing of transistors, the traditional elements used impose several challenges such as power dissipation, leakage and so on. These factors risk the cost efficiency of microsystems and risk the semiconductor industry's capability to prolong Moore's law in the nanometer range. This is overcome by the introduction of carbon materials such as nanosheet FET. They are advantageous over the traditional elements in terms of area and power efficiency. We design an energy and power efficient SoC with nanosheet FET that provides noise tolerance and memory optimization.

Keywords: System on Chip, Nanosheet FET, TCAD, Low power SoC, Memory optimization

1. INTRODUCTION

There has been remarkable progress in the semiconductor industry over the recent past. Integrated circuits are becoming more complex and costly. Impressive densities are achieved in Very Large Scale Integrated (VLSI) Circuits. In order to keep up with the integration levels, new methods are established to cope up with the complexity in large chips. For this purpose, industries are adapting new designs and reuse methodologies. System-on-Chip (SoC) design is one such technology where prefabricated and pre-verified blocks collectively known as intellectual property (IP) blocks, virtual components or IP cores are combined to form a single chip. This SoC/IP approach can be used to achieve high productivity gain. SoC designers work towards integrating these components into a single chip to implement advanced functions in a short span of time. It can be viewed as transferring a multichip system-on-board (SoB) to a single chip encompassing digital logic, RF blocks, analog/mixed signal and memory. The driving factors for this development are power reduction, reduced form factor and reduced cost.

In realising SoC, the main hitch includes fabrication complexity due to the process variation between transistors and memories. Lee et al. [3] used simple atomic force microscope lithography to fabricate switching as well as memory devices by creating narrow graphene oxide (GO) barriers in single layer graphene at measured oxidation voltages. The graphene component with non-volatile resistive switching can be cast-off as memory element and device with high on/off Fowler-Nordheim Tunnelling (FNT) current can be used as transistor element. This fabrication methodology has led to extensive usage of graphene SoC.

The use of nanometer technology makes it progressively significant to contemplate reliability issues during the design of communication architectures using SoC [9]. As technology scaling is done in the nanometer range, the energy consumption and delay of global interconnect structure causes glitches in the SoC design.

2. RELATED WORK

In the current nanoelectronics era, design of SoC creates several opportunities as well as challenges. More than a billion transistors are estimated to be assimilated on a single chip incorporating numerous semiconductor intellectual property (IP) blocks and custom-made processing units (PUs) [12]. Performance deprivation and synchronization glitches occur between the IP blocks as wire delays are more critical than the gate delays [13]. Yoon et al. [5] analysed V_{th} discrepancies of the 7-nm node NSFETs by diverse work functions of the work function metal established on a TCAD platform standardised with 10-nm node FinFETs in terms of device organisation and efficiency.

Lee et al. [6] suggested the need to study both digital as well as analog and radio frequency performance of Stacked Nanosheet Field Effect Transistor (SNSH-FET) in SoC applications. The flexibility of using stacked channel FET in SoC can be realized in perpendicularly stacked channel based unified memory, which is a combination of DRAM and flash memory on a single transistor. Jegadheesan et al. [7] display the flexibility of cell radio tuning for SoC applications by computing the influence of nanosheet width and thickness on DC performance of SNSH-FET. Samsung Electronics has acknowledged the launch of 3nm gate nanosheet transistors around the year 2022 [18].

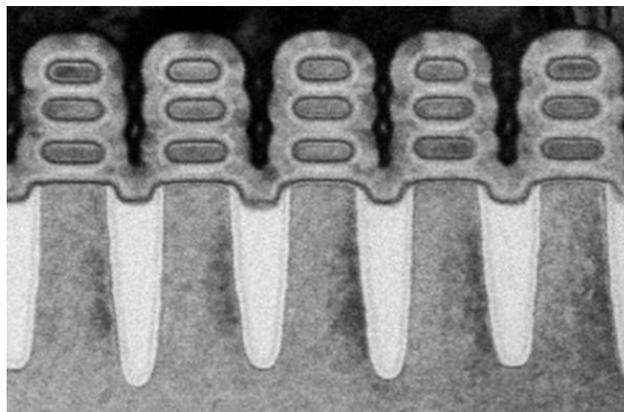


Figure 1 Samsung Nanosheet Transistors [18]

Kyunghee et al. [15] developed a two dimensional modulated MoS_2 FETs by directly imprinting MoS_2 flakes on the nanosheet transistor gate structure. Yakimets et al. [16] worked on a comparison of 3 piled nanosheets of 20nm that are competitive in comparison to FinFETs with 2 fins when the layout design rules are relaxed. The power optimization and frequency gain along with area scaling varies for every technology. Nanosheet FET offers improved gate control for low V_{DD} , adjustable device width and design tractability.

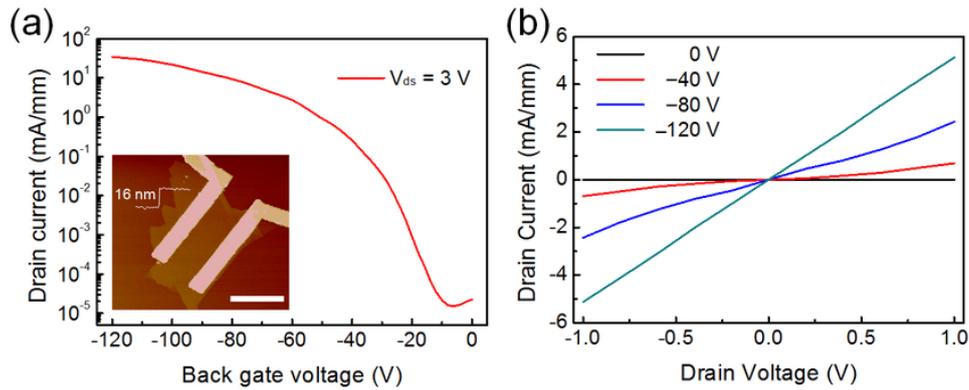


Figure 2 Transfer Characteristics of Nanosheet FET [17]

3. PROPOSED WORK

Formerly, FinFETs were commonly used as low power transistors. With advancement in technology, FinFETs were tried to be scaled down. But there was a leakage current that was produced [1]. Hence nanosheet FETs (NSFETs) are used. It is proved to be efficient in small dimensions when compared to FinFETs. Sentaurus TCAD software is used for the simulation of NSFETs [2]. The nanosheet width of NSFETs can be effortlessly adjusted. This allows flexible cell design for power and efficiency optimization [4].

3.1 Reliable SoC Design Architecture

We design a SoC based on two factors namely, system-level consistency and energy efficiency. Reliability can be accomplished by generating a signal power that is greater than noise. However, this methodology is particularly incompetent in terms of energy consumption. For decreasing this energy consumption, nanosheet FETs are used.

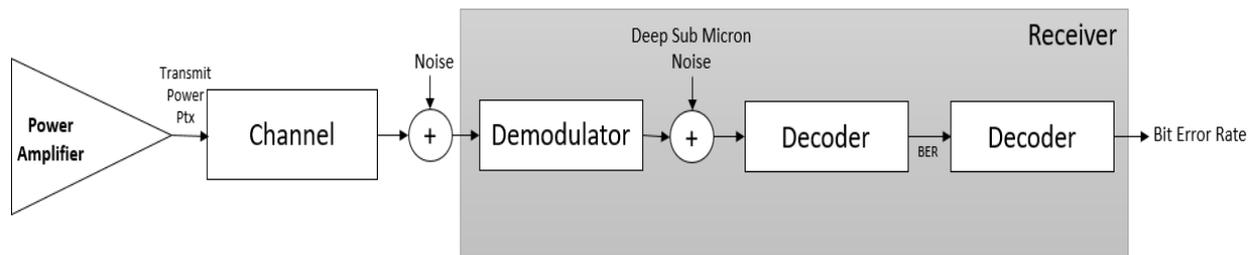


Figure 3 Communication Channel Module

The communication channel module shown in figure 3 comprises of a power amplifier that transmits power to the channel. This transmitted power is combined with noise signals and fed to the receiver unit that comprises of demodulator and decoders. The demodulator output is exposed to deep submicron noise signals which is further fed to the first stage decoder. The use of multiple decoders help in reducing the bit error rate and correction of the error signals.

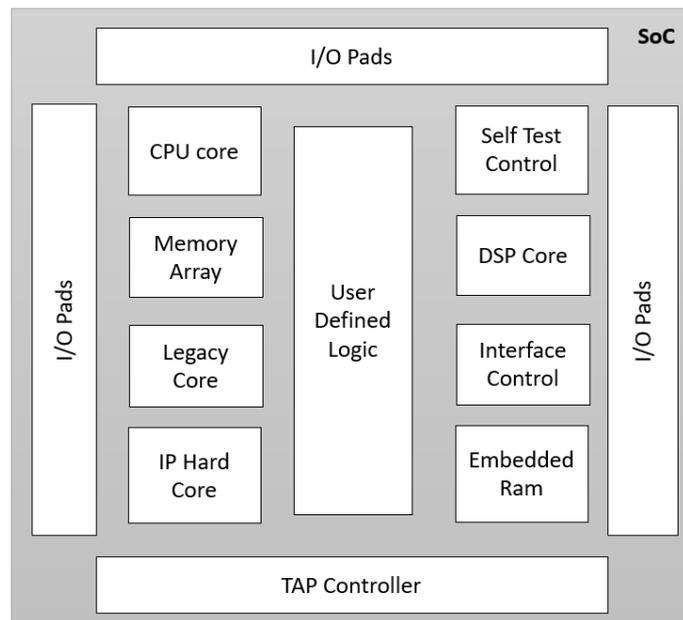


Figure 4 Structure and IP Blocks of SoC

3.2 Energy and Power Efficiency

With the increase in clock frequency and reduction in feature size, the global wire delays cause synchronization issues. Process ambiguity and electrical instabilities that may result in transmission errors influence the global interconnections that cover the whole chip area [11]. Major share of overall system power budget is consumed by the IP intercommunication. Accommodating these communication necessities and proficient interconnection of predefined and verified IPs decide the performance of SoCs.

While considering vertical nanosheet design, factors such as parasitic capacitance and resistance throughout the device are to be considered. Rather than single inverter, self-driven systems such as Ring Oscillator (RO) provides lesser concerns regarding input slew rate [8]. Hence the comparison of efficiency becomes slightly complicated as we cannot choose between input signal and the load. For a SoC critical path, an RO can be considered a satisfactory proxy if fan-out and back end of line (BEOL) are selected accurately.

3.3 Noise Tolerance

Pricey packaging schemes and sophisticated power management systems are introduced to handle this noise and power discrepancies. Upsurge in noise and power variations leads to challenges in designing consistent and effective computing system with nanometer processes [10]. Scaling of feature sizes in sub-100nm scale and

3.4 Memory Optimization

The memory compatibility chart has to be segregated in groups in order to reduce the total expense and thereby attain an efficient system-level distribution of memory elements. As the number of memory banks and interfaces increases, the critical path is affected. Hence, while designing the process, it is essential to establish a restraint to the volume of memory sharing.

We realize an algorithm that can accommodate the classification of all processor and deal with constraints such as bandwidth enforced by memories that are designated for specified technologies. We can thereby determine the establishment of memory subsystems in terms of multibank architecture that can satisfy certain constraints while reducing the memory footprint by reusing the memory banks. A configurable memory controller that can deal with the combined requirements of all processes as well as the memory is used by the algorithm.

3.5 Software Development Environment

The design flow of a SoC involves 5 steps inclusive of system specification, architectural exploration, software design, hardware design, and hardware-software integration. The application software are organized by software developers as a stack of layers executing on each processor core. A hardware abstraction layer is used by the software designers since the final hardware platform will not be available while developing the software. We use the description language SpecC [14] that uses extended C programming. Virtual architecture and service access ports (SAPs) are used for co-designing the hardware and software content.

4. RESULT

A noise tolerant energy and power efficient SoC has been developed with Nanosheet FET overcoming the difficulties of traditional transistor materials on scaling in the nanometer range. The RC delay is reduced in nanosheet FET when compared to CMOS. These materials offer better switching current and resistance based on oxidation voltages. Noise tolerance and memory optimization features are also considered in the design of the

SoC. Using the same process for the manufacture of both transistor and memory element also improves the efficiency of the device.

5. CONCLUSION AND FUTURE WORK

The Nanosheet FET based SoC offers better performance and versatility when compared with the traditional FET used in SoC. The noise ratio is limited as the graphene material used allows low leakage. It provides area and power optimization. Also, the development of all the IPs using Nanocarbon structures shows a tremendous improvement in the efficiency of the SoC device. Future work involves fabrication of individual IP blocks with nanocarbon materials so as to improve the density of SoC thereby increasing the complexity and performance of the device.

References

- [1] Auth, Chris, A. Aliyarukunju, M. Asoro, D. Bergstrom, V. Bhagwat, J. Birdsall, N. Bisnik et al. "A 10nm high performance and low-power CMOS technology featuring 3 rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects." In 2017 IEEE International Electron Devices Meeting (IEDM), pp. 29-1. IEEE, 2017.
- [2] Sentaurus, T. C. A. D., and G. Version. "Synopsys Inc." Mountain View, CA (2008).
- [3] Lee, Duk Hyun, Cheol Kyeom Kim, Jun-Ho Lee, Hyun-Jong Chung, and Bae Ho Park. "Fabricating in-plane transistor and memory using atomic force microscope lithography towards graphene system on chip." Carbon 96 (2016): 223-228.
- [4] Barraud, S., V. Lapras, B. Previtali, M. P. Samson, J. Lacord, S. Martinie, M-A. Jaud et al. "Performance and design considerations for gate-all-around stacked-nanowires FETs." In 2017 IEEE International Electron Devices Meeting (IEDM), pp. 29-2. IEEE, 2017.
- [5] Yoon, Jun-Sik, Jinsu Jeong, Seunghwan Lee, and Rock-Hyun Baek. "Multi-Vth Strategies of 7-nm node Nanosheet FETs with Limited Nanosheet Spacing." IEEE Journal of the Electron Devices Society 6 (2018): 861-865.
- [6] Lee, Byung-Hyun, Dae-Chul Ahn, Min-Ho Kang, Seung-Bae Jeon, and Yang-Kyu Choi. "Vertically integrated nanowire-based unified memory." Nano letters 16, no. 9 (2016): 5909-5916.

- [7] Jegadheesan, V., K. Sivasankaran, and Aniruddha Konar. "Impact of geometrical parameters and substrate on analog/RF performance of stacked nanosheet field effect transistor." *Materials Science in Semiconductor Processing* 93 (2019): 188-195.
- [8] COLLAERT, NADINE, and ANDA MOCUTA. "Built-In Sheet Charge as an Alternative to Dopant Pockets in Tunnel Field-Effect Transistors."
- [9] Raghunathan, Vijay, Mani B. Srivastava, and Rajesh K. Gupta. "A survey of techniques for energy efficient on-chip communication." In *Proceedings of the 40th annual Design Automation Conference*, pp. 900-905. ACM, 2003.
- [10] Shanbhag, Naresh R. "Reliable and efficient system-on-chip design." *Computer* 37, no. 3 (2004): 42-50.
- [11] Lee, Kangmin, Se-Joong Lee, and Hoi-Jun Yoo. "Low-power network-on-chip for high-performance SoC design." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 14, no. 2 (2006): 148-160.
- [12] Semiconductor Industry Association. "International technology roadmap for semiconductors." [Http:// www. Itrs. Net](http://www.Itrs.Net) (2009).
- [13] Dally, William J., and Brian Towles. "Route packets, not wires: on-chip interconnection networks." In *Proceedings of the 38th annual Design Automation Conference*, pp. 684-689. Acm, 2001.
- [14] Cesário, Wander O., Damien Lyonnard, Gabriela Nicolescu, Yanick Paviot, Sungjoo Yoo, Ahmed A. Jerraya, Lovic Gauthier, and Mario Diaz-Nava. "Multiprocessor SoC platforms: a component-based design approach." *IEEE Design & Test of Computers* 19, no. 6 (2002): 52-63.
- [15] Choi, Kyunghye, Young Tack Lee, Sung-Wook Min, Hee Sung Lee, Taewook Nam, Hyungjun Kim, and Seongil Im. "Direct imprinting of MoS₂ flakes on a patterned gate for nanosheet transistors." *Journal of Materials Chemistry C* 1, no. 47 (2013): 7803-7807.
- [17] Yakimets, D., M. Garcia Bardon, D. Jang, P. Schuddinck, Y. Sherazi, P. Weckx, K. Miyaguchi et al. "Power aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology." In *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 20-4. IEEE, 2017.

[18] Qin, Jingkai, Gang Qiu, Jie Jian, Hong Zhou, Lingming Yang, Adam Charnas, Dmitry Y. Zemlyanov et al. "Controlled growth of a large-size 2D selenium nanosheet and its electronic and optoelectronic applications." *ACS nano* 11, no. 10 (2017): 10222-10229.

[19] <https://www.eenewsanalog.com/news/samsung-introduce-nanosheet-transistors-3nm-node-0/page/0/1>

[20] Rodder, Mark S., Borna Obradovic, Rwik Sengupta, Dharmendar Reddy Palle, and Robert C. Bowen. "Integrated circuits with Si and non-Si nanosheet FET co-integration with low band-to-band tunneling and methods of fabricating the same." U.S. Patent 9,287,357, issued March 15, 2016.

[21] Hills, Gage, Marie Garcia Bardon, Gerben Doornbos, Dmitry Yakimets, Pieter Schuddinck, Rogier Baert, Doyoung Jang et al. "Understanding energy efficiency benefits of carbon nanotube field-effect transistors for digital VLSI." *IEEE Transactions on Nanotechnology* 17, no. 6 (2018): 1259-1269.

[22] Chen, Hung-Bin, Yung-Chun Wu, Chun-Yen Chang, Ming-Hung Han, Nan-Heng Lu, and Ya-Chi Cheng. "Performance of GAA poly-Si nanosheet (2nm) channel of junctionless transistors with ideal subthreshold slope." In *2013 Symposium on VLSI Technology*, pp. T232-T233. IEEE, 2013.

[23] Jiang, Zhi, Yang Wang, Shuoguo Yuan, Lu Shi, Ni Wang, Jie Xiong, Wenhui Lai et al. "Ultrahigh-Working-Frequency Embedded Supercapacitors with 1T Phase MoSe₂ Nanosheets for System-in-Package Application." *Advanced Functional Materials* 29, no. 9 (2019): 1807116.