Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

DESIGN AND ANALYSIS OF LOW-POWER, HIGH-SPEED BAUGH WOOLEY MULTIPLIER

Dr. P. Karuppusamy,
Professor, Department of EEE,
Shree Venkateshwara Hi-Tech Engineering College,
Erode, India.
Email id: pkarrupusamyphd@gmail.com

Abstract: The fundamental operations of the communication are the multiplication and division. The multiplier usually consumes a larger area and power and poses a very high latency. As all the above mentioned characteristics of the multiplier depends on the techniques utilized for the multiplication. It becomes necessary to put into effect a proper multiplier that reduces both the latency and the power consumption. So the paper analysis the performance of the various multipliers and scopes to develop a low power high speed multiplier based on the Baugh Wooley algorithm. The Performance analysis of the Baugh Wooley multiplier and the other existing multipliers is done and was found that the performance of the Baugh Wooley in terms of the latency and the power consumption was convincing compared to the other existing methods.

Keywords: Multiplier, Wallace multiplier, booth multiplier, Baugh Wooley multiplier**,** Xilinx simulation tool

1. INTRODUCTION

The multipliers [1-3] and the adders have a significant role in the variety of the systems that are used in the communication as well as the signal processing as they serve as the fundamental components of the computational circuits. Most of the digital circuits that are utilized in the signal processing applications and the VLSI systems engage the multiplier circuit. As the techniques used in the multiplication operation consumes most of the power allotted for the computation. It becomes necessary develop a multiplier that consumes low power and operates at a high speed[4-8].

The development of the multipliers has ensured a significant enhancement in the applications associated with the signal processing and the communication; the multipliers are utilized in the many roles not excluding the process of filtering, spectral analysis etc. As most of the applications of the communication and the digital signal processing nowadays aim at a mobile system that are battery-operated, the power consumption becomes the one of the basic design limitation[9-12]. In the meantime the multipliers that take a significant role in these application are a

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

complex frame work and operate at a high system clock rate, reducing the delay of the multiplier is a very tedious task as the overall design has to be satisfied.

As the speed of the computation in the signal processing as well as the communication depends mainly on the speed of the multipliers it also become necessary to develop a multiplier that operates at a high speed. The fig.1 below shows the classification of the multipliers.

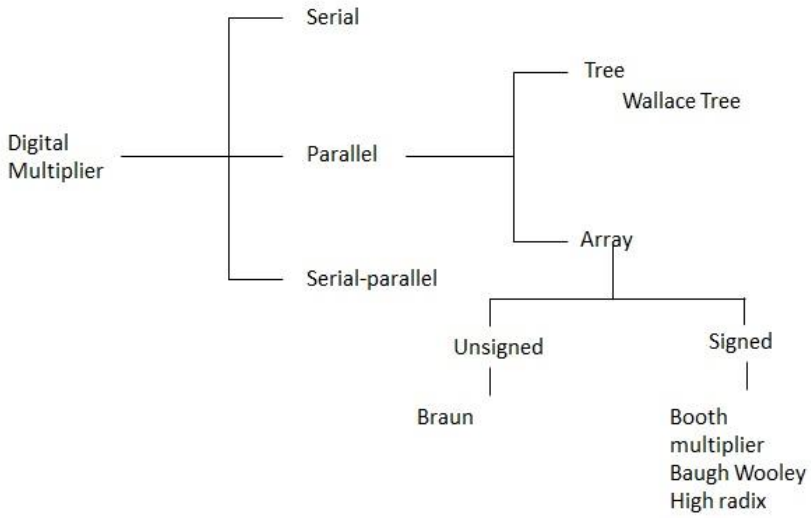


Fig.1 Types of Multipliers

The paper puts forth the low power high speed, multiplier circuit by modifying the addition process to thereby reduce the power consumption and increase the speed of the multiplier by decreasing the delay in the process. The paper is organized with the existing works in the section 2. The Proposed work in the section 3, the performance assessment in the section 4 and conclusion in the section 5.

2. EXISTING WORK [1-12]

The section holds the existing digital multipliers that are utilized for both the signed and the unsigned integers, some of the multipliers are the Braun, Booth, Baugh Wooley and the Wallace Tree multiplier. The parallel multiplier as shown in the fig .1 is classified into two types as the tree and array multiplier. The multiplier such as the Braun,

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

Booth, and Baugh Wooley comes under the array multiplier and the Wallace tree comes under the Tree multipliers. The Tabulation below in the table.1 shows the description merits and the demerits of the both the array and the tree type multipliers.

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

Parallel Multipliers	Categories	Description	Advantages	Disadvantages
Array	Braun	Braun Array multiplier is well known due to its regular structure. It is a simple parallel multiplier that is commonly known as carry save array multiplier. This multiplier is restricted to performing multiplication of two unsigned numbers. It consist of array of AND gates and adders arranged in iterative structure that does not require logic registers. This is also known as the non-additive multiplier since it does not add an additional operand to result of multiplication	Regular structure ,Easy to layout ,Small size ,The design time of an array multiplier is much less, Ease of design for a pipelined architecture.	Increase in the operand size increases the array size
	Booth	The Booth multiplier makes use of Booth encoding algorithm in order to reduce the number of partial products by considering two bits of the multiplier at a time, thereby achieving a speed advantage over other multiplier architectures. It is valid for both the signed and the unsigned numbers	Reduced delay	require large area of silicon, unlike the add-shift algorithms, which require less hardware and exhibit poorer performance
	Modified Booth	Recoding the multiplier in higher radix is a powerful way to speed up standard Booth multiplication algorithm. In each cycle a greater number of bits can be inspected and eliminated therefore, total number of cycles required to obtain products get reduced.	High Speed	require large area of silicon,
Tree	Wallace Tree	Wallace method uses three-steps to process the multiplication operation. ? Formation of bit products. ? The bit product matrix is reduced to a 2-row matrix by using a carry-save adder. ? The remaining two rows are summed using a fast carry propagate adder to produce the product.	High speed , medium complexity	Occupies large are a, and posses a irregular layout.

Table.1 Parallel Multipliers

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

3. PROPOSED WORK

The Baugh Wooley multiplier is the most effective method in computing the signed numbers; it was utilized in developing the regular multipliers that were more suited for the 2's complement numbers. It provides a high speed signed operation by using the parallel products to complement the multiplication process and regulate the partial products to enhance the adjustment in the multiplication array. For a number in its 2's complement format its sign is registered into the Baugh Wooley multiplier in order to keep partial product bits positive in turn to employ directly the addition techniques. For a two's complement multiplication the resulting partial product is obtained by performing the AND operation for the multiplier bit and the multiplicand bit, and the sign of the partial product is kept positive. The fig .2 below shows the Baugh Wooley Architecture.

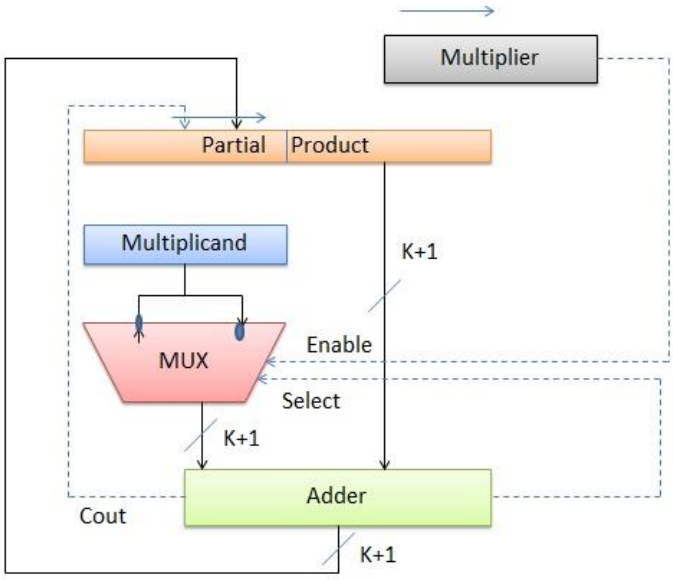


Fig .2 Baugh Wooley Architecture [15]

To enhance the speed by reducing the delay and improving the power consumption of the multiplier that is based on the Baugh Wooley architecture. A modified full adder circuit that is based on the CMOS domino logic [13] [14] is utilized in the multiplier. The circuit usually utilizes less area as a single active pull up is used and performs

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

operation using the series of a pre-charge and the valuation phase. The CMOS domino implemented in the full adder is shown in the fig .3 below.

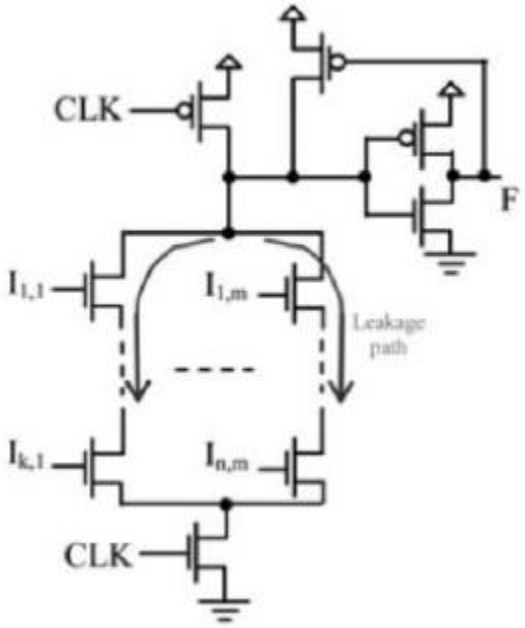


Fig.3 Modified Adder using Domino Logic [14]

The absence of the pull up network that is comprised of the PMOS enables the adders to exhibit a high switching speeds while occupying low area, this makes them to be highly utilized in many applications , the reduced area occupancy of the adder in turn reduces the size of the multiplier and the minimizes the delay. The minimized power consumption of the adder in turn brings down the overall power consumption of the multiplier circuit thus making the multiplier well suited for the low power high speed appliances.

4. PERFORMANCE ANALYSIS

ISSN: 2582-3825 (online)

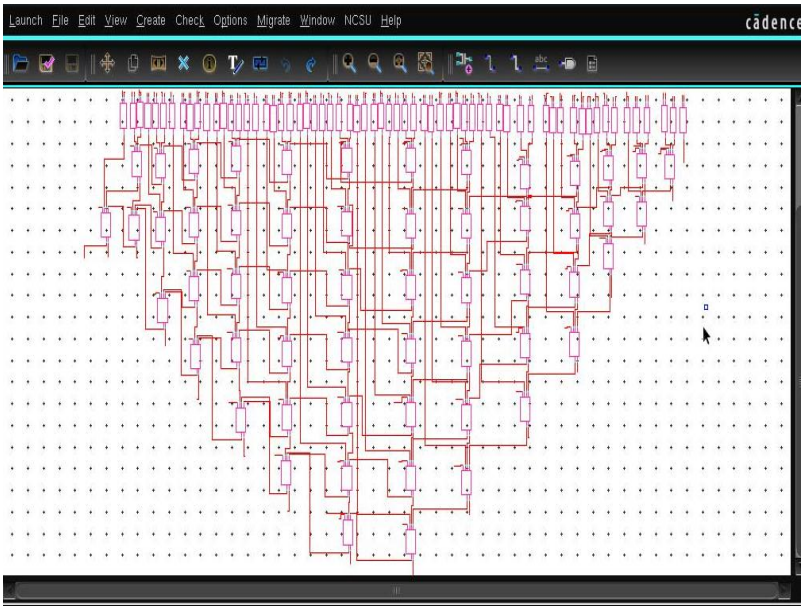
Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

The proposed Baugh Wooley multiplier with the modified adder circuit based on the domino logic is designed using the cadence virtuoso and simulated with the cadence Spectre by initiating an analog design environment. The table.2 below provides the details of the simulation parameter.

Simulation Parameter	Value
Environment	ADEL
Analysis Mode	Transient Analysis
Set Stop Time	100ns

Table.2 Simulation Parameters

The following figure.4 is the schematic of the Baugh Wooley utilizing the modified adder circuit designed in the cadence.



ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

Fig.4 Schematic of Baugh Wooley with the Modified Adder Circuit

The fig .5 below presents the transient response obtained for the multiplier circuit simulated with the cadence Spectre by initiating an analog design environment.

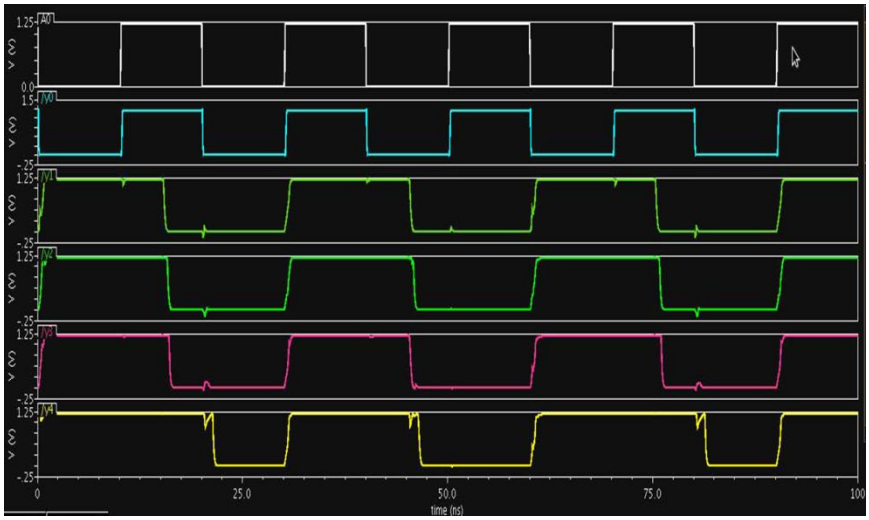


Fig.5 Transient Response of the Baugh Wooley with the Modified Adder Circuit

The table.3 below presents the power consumed and the delay encountered by the Baugh Wooley with the modified adder circuit and the exiting Baugh, Booth multiplier and the Wallace tree multiplier.

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

Input 1	Input 2	Baugh		Booth		Wallace		Baugh with the Modified Adder Circuit	
		Power (mw)	Delay (ns)	Power (mw)	Delay (ns)	Power (mw)	Delay (ns)	Power (mw)	Delay (ns)
00000000	00000000	.377	4.56	1.456	5.430	1.023	3.234	.211	2.05
10101011	11110000	.347	4.67	1.345	5.345	1.026	3.567	.234	2.56
00001111	11110000	.359	4.87	1.234	5.567	1.045	3.765	.204	2.78
11111111	11111111	.378	4.98	1.678	5.234	1.032	3.859	.252	2.67
10101110	11010101	.435	4.88	1.765	5.786	1.034	3.452	.231	2.89

Table.3 Comparison of Multipliers

The results obtained shows that the Baugh Wooley multiplier with the modified adder circuit shows a much reduced delay and power consumption compared to the other prevailing methods.

5. CONCLUSION

The multiplication playing the vital role in the digital signal processing and the communication consumes almost all the power that is allotted for the computation. So in order to have a high speed and a low power multiplier with a reduced power consumption and enhanced speed of the operation, the paper proposes the Baugh Wooley Multiplier with the modified adder circuit using the cadence virtuoso. The design is simulated using the cadence Spectre by initiating an analog design environment. The result obtained proves the competence of the Baugh Wooley Multiplier with the modified adder circuit in terms of the delay and power consumption when compared to the prevailing multipliers.

References

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

[1] Rao, Pachara V., Cyril Prasanna Raj, and S. Ravi. "Vlsi design and analysis of multipliers for low power." In *2009 Fifth International Conference on Intelligent Information Hiding and Multimedia Signal Processing*, pp. 1354-1357. IEEE, 2009.

[2] Khatibzadeh, Amir, and Kaamran Raahemifar. "A novel design of a 6-GHz 8/spl times/8-b pipelined multiplier." In *Fifth International Workshop on System-on-Chip for Real-Time Applications (IWSOC'05)*, pp. 387-391. IEEE, 2005.

[3] Khatibzadeh, Amir Ali, Kaamran Raahemifar, and Majid Ahmadi. "A 1.8 V 1.1 GHz novel digital multiplier." In *Canadian Conference on Electrical and Computer Engineering, 2005.*, pp. 686-689. IEEE, 2005.

[4] Prabhu, A. S., and V. Elakya. "Design of modified low power booth multiplier." In *2012 International Conference on Computing, Communication and Applications*, pp. 1-6. IEEE, 2012.

[5] Kakde, Sandeep, Shahebaj Khan, Pravin Dakhole, and Shailendra Badwaik. "Design of area and power aware reduced Complexity Wallace Tree multiplier." In *2015 International Conference on Pervasive Computing (ICPC)*, pp. 1-6. IEEE, 2015.

[6] Gomes, Savio Victor, P. Sasipriya, and VS Kanchana Bhaaskaran. "A low power multiplier using a 24-transistor latch adder." *Indian Journal of Science and Technology* 8, no. 18 (2015): 1-5.

[7] Senthilpari, C., K. Diwakar, and Ajay Kumar Singh. "High speed and high throughput 8× 8 bit multiplier using a Shannon-based adder cell." In *TENCON 2009-2009 IEEE Region 10 Conference*, pp. 1-5. IEEE, 2009.

[8] Khan, Shahabaz, Sandeep Kakde, and Yogesh Suryawanshi. "Performance analysis of reduced complexity Wallace multiplier using energy efficient CMOS full adder." In *2013 International Conference on Renewable Energy and Sustainable Energy (ICRESE)*, pp. 243-247. IEEE, 2013.

[9] Keerthana, L., and M. Nisha Angeline. "VLSI Design and FPGA Implementation of N Binary Multiplier Using N-1 Binary Multipliers."

[10] Bibi, Safia, Muhammad Obaid Ullah, and Muhammad Ali Shami. "Design and analysis of hybrid tree multipliers for reduction of partial products." *Mehran University Research Journal of Engineering and Technology* 37, no. 3 (2018): 483-492.

[11] Kumar, KS Ganesh, J. Deva Prasannam, and M. Anitha Christy. "Analysis of low power, area and high speed multipliers for DSP applications." *International Journal of Emerging Technology and Advanced Engineering* 4, no. 3 (2014).

[12] Fritz, Christopher, and Adly T. Fam. "Interlaced Partition Multiplier." *IEEE Transactions on Computers* 65, no. 8 (2015): 2672-2677.

[13] Verma, Shekhar, Dhirendra Kumar, and Gaganpreet Kaur Marwah. "New high performance 1-bit full adder using domino logic." In *2014 International Conference on Computational Intelligence and Communication Networks*, pp. 961-965. IEEE, 2014.

ISSN: 2582-3825 (online)

Journal of Electronics and Informatics (2019)
Vol.01/ No. 02
Pages: 60-70
http://www.irojournals.com/iroei/
DOI: https://doi.org/10.36548/jei.2019.2.001

[14] Halder, Mousam. "Implementation of high speed low power carry look ahead adder using Domino logic." *International Journal of Applied Sciences and Engineering Research* 1, no. 3 (2012): 446-451.

[15] Warrier, Rakesh, Chan Hua Vun, and Wei Zhang. "A low-power pipelined MAC architecture using Baugh-Wooley based multiplier." In *2014 IEEE 3rd Global Conference on Consumer Electronics (GCCE)*, pp. 505-506. IEEE, 2014.

ISSN: 2582-3825 (online)