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Transistor Sizing using Hybrid Reinforcement Learning and Graph Convolution Neural Network Algorithm

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Abstract

Transistor sizing is one the developing field in VLSI. Many researches have been conducted to achieve automatic transistor sizing which is a complex task due to its large design area and communication gap between different node and topology. In this paper, automatic transistor sizing is implemented using a combinational methods of Graph Convolutional Neural Network (GCN) and Reinforcement Learning (RL). In the graphical structure the transistor are represented as apexes and the wires are represented as boundaries. Reinforcement learning techniques acts a communication bridge between every node and topology of all circuit. This brings proper communication and understanding among the circuit design. Thus the Figure of Merit (FOM) is increased and the experimental results are compared with different topologies. It is proved that the circuit with prior knowledge about the system, performs well.

Keywords: Transistor Sizing, Graph Convolutional Neural Network (GCN), Reinforcement Learning (RL), Figure of Merit (FOM), Nodes and Topology.

1. Introduction

The automatic transistor sizing is one of the attractive segments in VLSI designing. In most cases analog circuit is designed by many researchers but due to its designing area, time and trade-off it is a complex process to be accomplished by a specific tool. It requires huge

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manpower and the built-in procedure is expensive. An individual can't design these circuits easily because there is a need for deep analysis to meet the expected performance [1]. Since it is non-linear in nature we have to analyse and understand the topology of the circuit before starting the designing procedure. The entire design procedure requires immense computations, equations, simplification and approximations. The initial stage is designed with raw calculation and then, by making some correction to the initial stage the circuit is fine-tuned [2]. Then the obtained parameters are carried to the simulation tool to get optimized. This makes huge demand of manpower, production cost and labour charge. In parallel it consumes more time to complete the process. To reduce the design area, cost and time we move towards automatic transistor sizing [3]. Due to the transistor scaling we need to transfer port information from one node to another. In practice it is a difficult process to check and update each and every time. Many experiments have been conducted to sort this issue. But fixing it within one circuit is quite difficult to accomplish and many researchers are trying to achieve this [4]. In this proposed work, the learning capability of reinforcement learning is utilized to accomplish this task. Initially in the training phase, a single circuit was considered and a RL agent was implemented to transfer the information among the nodes in that specific circuit. After the training process the same RL agent was implemented to all topologies in the circuit to transfer the information. Thus it reduces the cost for simulation while designing [5].

Initially the transistor sizing is meant to be a black-box optimization issue and many traditional optimization methods such as Bayesian Optimization, Evolutionary Strategy and so on was used to resolve this issue but wasn't able to achieve the expected results successfully [6]. In this proposed method the black-box issue is brought into a loop and the circuit is considered as a graphical structure and graph convolutional neural network was implemented to fix this issue [7]. The RL agent is combined with this process to transfer the learning process between the topologies and nodes in the circuit. The performance of the system increases when each technical node knows each other and likewise the topological nodes knows each other [8]. The experimental results prove that the combined method of graph convolutional neural

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network and RL agent performs better than the Bayesian Optimization (BO) and Evolutionary Strategy (SE) methods [9].

The working procedure of the clout of graph convolutional neural network along with reinforcement learning method is given below.

a. Open-box optimization: The circuit is designed as per the topological parameter of the graph using GCN so that it enhances the performance of the system.

b. Applying RL: After optimizing the circuit the reinforcement learning algorithm is implemented. This enhances the performance of the system and thereby reduces the human error and black-box issue faced by the optimization methods.

c. Transferring the knowledge information: To simplify the design and simulation cost this method is equipped by transferring the information to topological nodes and technical nodes among the circuit.

Moreover the proposal is followed by a detailed explanation about the related work in section 2, the methodology along with algorithm is briefed in section 3, the experimental results are given in section 4 and conclusion is elaborately explained in section 5.

2. Related Work

Various traditional methods were implemented to achieve transistor sizing and they are categorized into two types based on knowledge and optimization. The knowledge based method depends on human intervention and it is consuming process since they use existing equation and methodologies for design purpose [10]. While deriving existing equation to build the transistor size, deep analysis and immense knowledge is needed about the current technology and its usage. This process requires huge manpower, proper maintenance, periodic update, high labour charge and is time consuming [11]. Further the optimization method has two branches based on model and simulation. The optimization based on model requires human

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interventions to perform calculation whereas the simulation based method requires simulators to perform the task [12]. The performance of the system is enhanced using multiple simulators and repeating n number of simulations. These optimization methods label the transistor sizing as a black-box issue and try to overcome [13]. The optimization methods fail to weigh the information of topological graph and transferring the knowledge between the nodes of the circuit [14].

The reinforcement learning methods are used widely in many fields such as gaming, automation, robotics and graphical networks for designing [15]. The RL is transferable in nature and it is capable of learning and adjusting to the corresponding environment. The fundamental parameters of RL is utilized in this proposed work. The reinforcement learning method works better than the supervised method [16]. Reinforcement learning method is applicable in the developing fields such as automations since its learning and adopting nature is the major advantage of the RL method. To analyse the graphical data, the Graph Neural Network has been used [17]. It has many types such as GCN, GAN and so on. The GCN is used in the proposed work [18]. To reduce the workload, accelerators are used in GNN. The GCN method is used to replace simulator and enhance the performance of the distributed circuits. In this proposed work, the merits and fundamental parameters of GCN and RL are used to achieve transistor sizing [19].

3. Proposed Work

3.1 Problem Statement

The analog circuit with fixed topology causes transistor sizing issue and this is expressed as bound-constrain optimization,

$$\max_{y \in D^m} FOM(y) \tag{1}$$

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where y represents the bound course, m represents the sum of bound examines, D^m represents the planning area, FOM represents Figure Of Merit. The equation 2 represents the balanced number of the stabilised performance metric.

$$FOM = \sum_{n=0}^{N} w_i \times \frac{\min(m_n, m_n^{bound}) - m_n^{min}}{m_n^{max} - m_n^{min}} \; ; with\ specified\ spec\ value \quad (2)$$

where the performance metric is denoted by m_n, m_n^{max} and m_n^{min} are the boundary factor used to normalize the performance metric, m_n^{bound} denotes the upper bound factor, the weighing parameter w_i is used to adjust the n^{th} parameter, spec is the pre-defined specification and in some cases FOM is assigned to a negative value to meet the spec requirement. The general overview of GCN and RL architecture is represented in Figure.1.

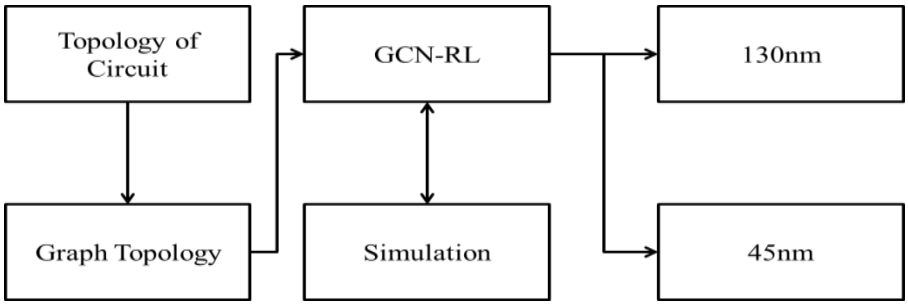

Figure 1. Block Diagram of GCN-RL

3.2 Overview of Framework

The working procedure of the framework is given below:

1. The circuit is considered as graph and their vertices and edges correspond to the components and wires respectively.
2. A state vector is created for every individual transistor and this is transferred to the RL agent via graph unit.
3. The RL agent assigns the action vector by examining each and every node in the circuit environment.

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4. Transistor matching is achieved by refining the action to a specific range and it is kept within its limit. The unwanted values are truncated and normalized to a rounded value.

5. Then we move on to the simulation.

6. Finally the FOM parameters are evaluated and updated to RL agent.

3.3 Formulation of Reinforcement Learning

The RL agent performs both model differentiation and picks the best performing point to a simulator.

State space: The step by step analysis is carried on the graph by RL agent and the state space is formulated as s_l = (l, t, v) where s_l represents the state and l represents the total component. T denotes the time taken and v denotes the selected vector. This differs for PMOS and NMOS transistor.

Action space: Based on the components the action space changes its nature.

a. For Resistor the action vector is $a_l^r = R$; R denotes the value of resistance

b. For capacitor the action vector is $a_l^c = C$; C denotes the value of capacitance

c. For PMOS & NMOS transistor the action vector is $a_l^{mos} = (w, i, m)$; w denotes the weight, the length of the gate is denoted by i and m denotes the multiplex.

3.4 GCN-RL Enhancement

The GCN process is used in each and every graphical topology unit of RL agent [20]. A single layer of GCN is capable of obtaining the hidden vector values of transistor. This is achieved by collecting information from neighbouring nodes. By combining all GCN layers

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[21] we can easily transfer information between nodes. 7 layers has been used in the proposed work. Each layer can communicate with its neighbours and the initial node has control over all the nodes. The general expression is given in equation 3

$$H^{j+1} = \sigma\left(\tilde{d}^{-\frac{1}{2}}\tilde{a}\tilde{d}^{-\frac{1}{2}}\right)H^{j}w^{j} \quad (3)$$

The RL agent's modelling and assigning features varies and the final outcome is normalized to obtain appropriate results. The DDPG is weighed to train the RL agent. The state and action are specified with its j^{th}digit and it is represented as s= {s_1, s_2….. s_m} and a= {a_1, a_2…..a_m}. The variance is reduced by taking the exponential moving average value of the last appeared reward. The noise and the unwanted values are truncated [22]. The RL agent is categorized into two types one with aggression and another without aggression of GCN. In this proposed work, aggression model of GCN is used.

3.5 Transferring Knowledge Information

The knowledge transfer is further divided into two types

a. Knowledge transfer between Topology of the circuit

b. Knowledge transfer between Technical nodes of the circuit

3.5.1 Knowledge Transfer between Topology of the Circuit

The RL agent is capable of transferring information between topologies of a circuit. We can even transfer information among the dual stage and tri stage of trans-impedance amplifier circuits. This is accomplished by utilizing the extracting features of GCN [23]. The state values are altered to enhance the performance of the system. Here it is altered from single hot index vector into 1-D index value. Only the state value is altered and the remaining parameters are kept same as the original value.

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3.5.2 Knowledge Transfer between Technical Nodes of the Circuit

The porting between technologies occurs due to transistor scale-off. An individual will inherit the technology of a single node and obtain the fundamental parameters from that node and then implement the same for entire design procedure which is followed by simulation. But in automatic method the entire process is automatically accomplished by the trained RL agent [24]. It is further used in the circuit with similar principles and architectural structure. It is capable to learn and understand the environment and act accordingly.

4. Result and Discussion

4.1 Comparative Results

To get a clear understanding and to show the performance of the system, this proposed work is compared with other existing traditional methods such as Dual-State Trans-impedance, Tri-State Trans-impedance, low dropout regulator and two-stage voltage amplifier [25]. A saleable 180nm TSMC is used in low dropout regulator and two-stage voltage amplifier and it is cadence is used as a simulator. The Dual-State Trans-impedance and Tri-State Trans-impedance amplifiers uses the same 180nm TSMC technology and Hspice simulator.

The Figure of Merit of this proposed work is compared with the two optimization techniques such as BO and SE. The data of BO and ES are obtained from an open-source and the results are compared. The Table.1 shows the comparative results of FOM.

Table 1. Performance Analysis of FOM

Method	Dual-TIA	Tri-TIA	Two-Volt	LDO
BO	2.67±0.04	1.92±0.03	1.31±0.04	0.41±0.08
ES	2.49±0.04	1.86±0.20	1.25±0.15	0.46±0.06
GCN-RL	2.70±0.04	2.24±0.12	1.42±0.02	0.80±0.03

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To enhance the significance, the experiment was repeated three times and the results are based on Equation 2. The boundary values are determined by sampling more than 6000 samples. The weighing values ranges from (-1, 1) to increase the performance and gain. The graphical representations of the comparative results can be visualized from Figure.2 and it is observed that the GCN performs more effectively and faster than other methods.

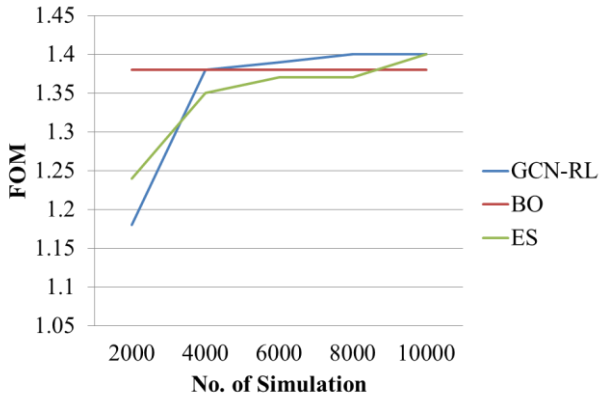

Figure 2. Graphical representation of GCN-RL performance

a. Duel-State Trans-Impedance

To convert the drain-current to drain-voltage, diode within the transistor is used as the output. The results are compared with the performance metrics (Gain, Bandwidth and Noise) and it is represented in table 2 and it is observed that the proposed method performs better than the other method and it satisfies the spec condition.

Table 2. FOM of Duel-State Trans-Impedance

Method	BW	GAIN	NOISE	FOM
ES	1.19	105	3.78	2.68
BO	0.17	124	1.69	2.52
GCN-RL	1.04	168	3.73	2.73

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The flexibility is determined by multiple repetitions of tests on performance metrics. The weight of the GCN is increased to leverage the performance metric. The spec value remains in a limit and for evaluation, the limitation of spec value is omitted. It is observed that this proposed method performs better than other methods in a faster manner.

b. Two-State Voltage Amplifier

To obtain stable PVT the amplifiers are connected in a closed loop and it is determined from the ratio of capacitor. The closed loop configuration is normalized by miller compensator. Here the CPM, DPM and the open loop gain is considered as performance metric. The comparative results are briefed in table 3.

Table 3. FOM of Two-state voltage amplifier

Method	CPM	GAIN	DPM	FOM
ES	181	51	4.44	1.94
BO	167	26	2.78	2.06
GCN-RL	181	30	9.64	2.34

c. Tri-state Trans-Impedance

To convert source current into voltage, input pair of common mode is used at the output. It is used as a booster circuit. The evaluation of performance metrics are detailed in table 1. It is observed that this method consumes minimal amount of power.

d. Low Dropout regulator

It is used to reduce the supply charge and to control the voltage. The FOM is briefed in table 1. It is observed that this posed method successfully achieves shortest settling time in both cases of load (increased load and decreased load).

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4.2 Transferring Knowledge among Technical Nodes

The experiments were conducted using RL agent trained by standard 180nm technology and it is further trained to a range of highest to lowest values such as (250 nm to 45nm). The trained RL agent is used to predict the parameter of Duel-State Trans-Impedance, Tri-state Trans-Impedance, Low Dropout regulator and Two-state voltage amplifier. The experiment is conducted over 300 samples and the results are observed in table 4.

Table 4. Knowledge Transfer between Technical Nodes

Method	45nm	65nm	130nm	250nm
Dual-TIA (without transfer)	2.37±0.07	2.37±0.10	2.44±0.04	2.37±0.06
Dual-TIA (with transfer)	2.52±0.05	2.53±0.05	2.57±0.03	2.56±0.02
Tri-TIA (without transfer)	0.54±0.06	0.56±0.04	1.66±0.15	0.70±0.26
Tri-TIA (with transfer)	1.07±0.08	1.21±0.10	1.30±0.06	1.28±0.03

4.3 Transferring knowledge among topology

Table 5. Knowledge Transfer between Topology

Method	Dual-TIA to Tri-TIA	Tri-TIA to Dual-TIA
Without transfer	0.64±0.08	2.38±0.02
NG-RL	0.63±0.10	2.41±0.08
GCN-RL	0.79±0.13	2.46±0.03

It is possible to transfer the knowledge among topology and Duel-State Trans-Impedance and Tri-state Trans-Impedance amplifiers were chosen because they belong to the same branch. The experiment aims to transfer the knowledge of Tri-state Trans-Impedance to

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dual state. For this purpose over 10000 steps were trained and converse experiments were conducted to check the stability and efficiency of the RL agent. The comparative results are tabulated in table 5 and it is graphically represented in figure.3.

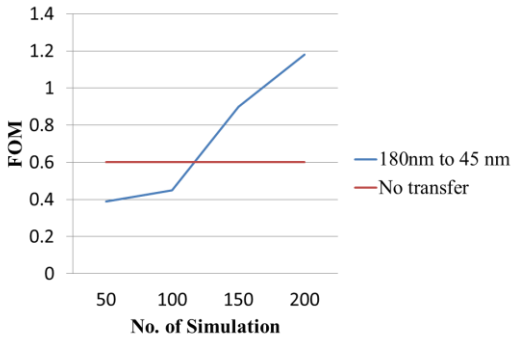

Figure 3. Graphical representation of GCN-RL Transfer ability

5. Conclusion

The ultimate aim is to achieve the transistor sizing and it is achieved by utilizing the convenient property of reinforcement learning. The RL agent is used to transfer knowledge information among technical nodes and topology of the circuit. This is accomplished by the intervention of graph convolutional neural network. By observing the experimental results it is evident that this proposed method has highest transferring property and has highest value of FOM. It is proved that this proposal serves as best platform to design circuit with transferring property. The combinational method of graph convolution neural network with Reinforcement Learning enhances the performance and effectively serves as port designer. Thus it is cost effective, reduces the time consumed by the simulator and individuals and faster than the previous methods.

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Author's biography

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