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A Review on Low Power VLSI Design Models in Various Circuits

S. Madhura

Department of Electronics and Communication Engineering, RV Institute of Technology and Management, Bangalore

E-mail: madhuras.rvitm@rvei.edu.in

Abstract

Low power design is one of the primary goals for any integrated circuits. Very Large-Scale Integration (VLSI) is a kind of Integrated Circuit (IC) that consists of hundreds and hundreds of transistor connection into a small chip. The communication and computer applications have grown very faster in the past decade due to the development of VLSI circuit design as microcontroller and microprocessors. However, still the research on VLSI are moving faster towards the scope of power and area minimization. The paper gives an overview about the recent methodologies that have been developed for the performance improvement of VLSI design and it shows the future directions of the areas that are to be concentrated on VLSI circuit design.

Keywords: CMOS, leakage power, transistor reduction, logic gates, low-power circuits

1. Introduction

Transistor miniaturization has reduced the power consumption of electronic circuits to certain extent but at the same time, it has improved the power density of the electronic circuits. The main challenge of designing a low power VLSI circuit is to maintain its computational power with reduced energy consumption [1]. Similarly, the circuits are designed to operate with more novel and unique features than its previous designs. This results in the development of powerful processors and that can be applied to data computing and computer vision applications. Hence it improves the power density in the VLSI circuit [2, 3].

To improve the performances of such circuit designs, certain design methodologies are followed in the present days for maintaining the scalability and reliability of the circuits without losing their nature. Figure 1 indicates the general merits of having a VLSI based

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circuit model. As low power devices are playing a major role in the enhancement of battery life, the VLSI circuits are implemented with hardware-based power maintenance system. Reduction of power consumption reduces the heat dissipation of the circuit and minimizes the space requirement for airflow in the circuit board [4]. The power consumption of a circuit can be controlled in two phases like active phase and standby phase.

- **Active phase:** The active phase power supply includes the power considered for the operation of the circuit. In general, it includes the power required for charging and discharging the transistor capacitance placed inside a VLSI circuit. Hence the VLSI circuits are implemented with CMOS logic for reducing the power consumption, and that is achieved by minimizing the switching operation on the operational stage.
- **Standby phase:** The standby power consumption represents the product of energy taken for the operation and the circuit leakage. The gate terminals of the transistor allow some current to leak over the circuit, and that creates heat dissipation in the circuit. Therefore, the bi-polar circuit designs are avoided in many cases.

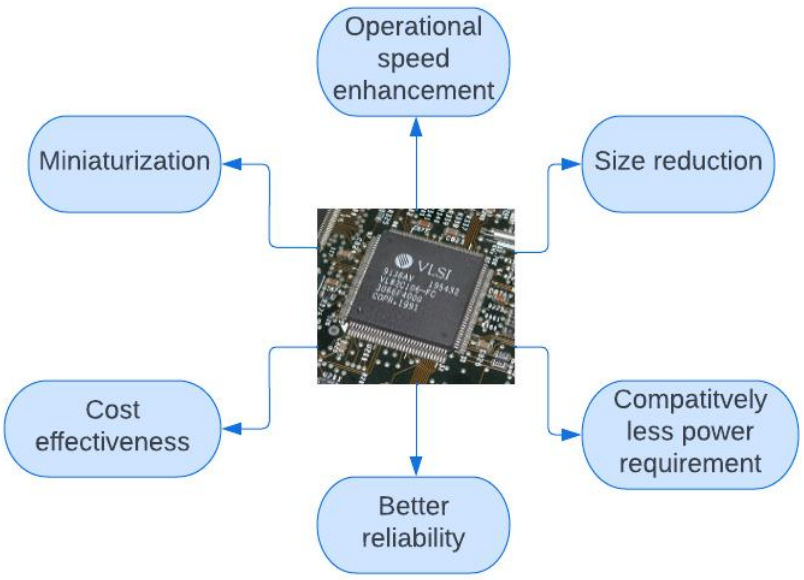

Figure 1. Merits of VLSI design

To limit the power consumption of VLSI circuits, the following modern techniques are implemented in many applications, and it can be implemented without any major change to the transistor logics [5].

1. **Voltage Scaling:** The power consumption of the circuits can be controlled by adjusting the logic level of the voltages in either of the direction. The power

consumption can be reduced by keeping the logic level to its minimum position on its switching phase.

2. **Frequency Scaling:** Similar to voltage scaling, the frequency outcome of the circuit can also be controlled in any direction based on its requirement. An optimum selection of frequency range will reduce the power leakage in a logic circuit.
3. **Clock Gating:** It helps to disconnect certain logic units from the circuit when it is not required for the operation, and that reduces the current leakage in the non-operated logic circuits.
4. **Bias Control:** The bias control technique is implemented along with the scaling methods, and that estimates the threshold for the voltage to be entered on the transistor. It is also represented as back scaling process when the voltage of CMOS is controlled during its operation with a threshold value.

The following section explores the list of recent methods that are developed to maintain low power consumption in VLSI designs.

2. Literature Survey

The demand for low power VLSI devices is increasing as the IC modules are placed in the places where the energy sources are not available. Applications like IoT and WSN require its system to be operated with very low power battery source. Table 1 explores the list of techniques that are developed to address the power requirement issue of VLSI modules in different applications.

Table 1. Survey on low power design methodologies

First author name & citation	Technique	Methodology	Application	Outcome
Kalavathi Devi [6]	Viterbi decoder utilizing a sleepy keeper method	Transistor leakage current control	WLAN	Avg. power Proposed = 0.85mW Existing power = 1.67mW
Singh [7]	Inverter logic	Transistor reduction	Hybrid full adder	Avg. power = 6.889µW

Kumar [8]	NMOS Stacking	Leakage current reduction	45nm CMOS VLSI circuit	21.97µW power difference over VCDG technique
Vidhyadharan [9]	Dynamic comparator design	Transistor ON-OFF control	Gate Overlap Tunnel FET	Avg. power Proposed = 1.11pW CMOS = 154pW
Tirumalasetty [10]	Pass transistor and transmission gate logic	Transistor count reduction	Hybrid 1 bit full adder	Leakage power Proposed = 1.68nW CMOS = 1.82nW
Vidhyadharan [11]	4T-STI based Ternary SRAM design	Avoiding direct path between supply and ground	32nm and 45nm VLSI application	Avg. power Proposed = 0.066 µW SWSFET = 2.6 µW
Barla [12]	Logic-in-memory architecture	Transistor reduction	Arithmetic logic unit	Avg. power Proposed = 187.7nW M-MALU = 262.3nW
Amini-Valashani [13]	Inverter logic modification	Feedback loop	Hybrid full adder	Avg. power Proposed = 3.79µW Hybrid CMOS = 14.32µW
Vidhyadharan [14]	Logic circuit based on Gate-Overlap Tunnel FET	Transistor ON-OFF control	Half adder	Avg. power Proposed = 1.26 µW CMOS = 2.69µW
Cai [15]	18TSPC topology	Transistor reduction	Single-phase flip-flop	27% of lower leakage current over TGFF
Thamaraimanalan [16]	Delay-based power gating technique	Transistor ON-OFF control	Adders and multipliers	Leakage power on (16 bit adder): Proposed = 98.65 µW

				Without control = 114.69 µW (4x4 array multiplier) Proposed = 80.26 µW Without control = 96.46 µW
Thangavel [17]	Sleepy keeper technique	Holding the actual logic state	Viterbi decoder	Avg. power Proposed = 73.84 µW CMOS design = 104.98 µW
Sowmya [18]	Multiple logic operation	Transistor reduction	Full adder	Avg. power Proposed = 41.91 µW Existing = 21.24 µW
Elango [19]	FFT and IFFT	Transistor logic utilization	MIMO-OFDM	Avg. power Proposed = 6.18 mW Existing = 8.19 mW
Razavi [20]	Markov random field	Logic state optimization	Low power VLSI circuit	Avg. power Proposed = 553.59 pW Existing = 1129.8 pW

3. Discussion

Transistor count reduction and transistor logic control are found to be the popular techniques used for reducing the power utilization on VLSI circuits. In very rare case, routing and optimization -based control techniques are found [6]. Similarly, all the proposed techniques are compared over the traditional CMOS methodology for analyzing their performance improvement [4, 5]. In some cases, the transistor logics are controlled using optimization method and path controlling strategy. A sleepy keeper technique was found by adding more number transistor to maintain the logic state of the previous transistor [12]. These kinds of methods reduce the power consumption, but improve the area required for the VLSI circuit. However, a good VLSI circuit design must compromise the area requirement and heat dissipation along with the reduced power consumption method.

4. Conclusion

VLSI circuits are developed to operate most complex arithmetic operations by adding more transistors and logic circuits in a microchip. The VLSI microchips are present in a normal calculator to a most advanced neural network-based application. Therefore, the continuous and heavy operations improve the power requirement of such circuits. The larger power consumption also causes the microchips to produce more heat than the usual operation. Hence several operational logics are introduced day by day to optimize the power consumption of the VLSI circuits. The paper summarizes the recent methods that are designed to minimize the power consumption of the VLSI chips, and it is found that the transistor reduction technique is the most utilized technique on saving the power. But to prove the efficiency of a developed technique, it must be compared over the recently developed design performance. Moreover, the study has determined a drastic performance difference between the simulation and physical experiments. The physical experiments show a slight variation in negative side over the simulation setup.

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Author's biography

S. Madhura was born in Bangalore, Karnataka, India. She received PhD in video processing from Visveswaraya Technological University in 2018. M.Tech degree from MSRIT, Bangalore in 2011. She is currently working as Assistant Professor in Department of Electronics and Communication in RV Institute of Technology and Management, Bangalore. She has teaching experience of more than 9 years with research experience of 7 years. Her research area includes Digital Signal Processing, Digital Circuits and Video/ Image processing.