

Camera Interfacing with FPGA for IC Segregation

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Abstract

This research introduces a ground breaking approach for the segregation of Integrated Circuits (ICs) using FPGA (Field Programmable Gate Arrays) -based automation. The proposed system integrates mechanical and digital components to efficiently orient, sequence, identify, and classify ICs, thereby streamlining the segregation process. Key features include orientation rectification using a vibrator-like model to ensure proper IC alignment, and sequencing through a servo motor-controlled conveyor belt that organizes the ICs systematically. Identification of ICs is achieved through image capture coupled with Sobel edge detection, allowing precise recognition of different IC types. Classification is then performed using a servo motor-controlled funnel to accurately sort the ICs into designated categories. The FPGA orchestrates the control of these components, ensuring seamless coordination and enhancing the efficiency and accuracy of the IC segregation process. This innovative system promises significant improvements in the automation and speed of IC segregation, reducing manual intervention and error rates.

Keywords: Conveyor, Sobel, Orientation, Segregation, Classification.

1. Introduction

The segregation of Integrated Circuits (ICs) is a critical aspect of electronics manufacturing and testing processes, ensuring that each IC is correctly identified and routed

for testing. Manual segregation methods are not only time-consuming but also prone to errors, highlighting the need for automated solutions. In response to this, our work presents a comprehensive FPGA (Field Programmable Gate Arrays) -based system for IC segregation, integrating mechanical and digital components to streamline the process. Our system comprises several key components, each serving a specific purpose in the segregation workflow. Firstly, an orientation rectification mechanism utilizes a vibrator-like model driven by a DC motor to tilt ICs, ensuring their proper orientation for classification. Next, an IC sequencing mechanism employs a conveyor belt controlled by a DC motor to deliver ICs one by one to a region where their images are captured for further processing. The core of our system lies in the IC identification process, where an OV7670 camera module captures the top surface of each IC as it reaches a transparent dropper stand. The FPGA, specifically an Altera DE1 board, is utilized to interface with the camera for image processing. This involves developing Verilog code for modules such as asynchronous FIFO, dual port sync, I2C master, and debounce explicit, which are simulated using Altera ModelSim software. Furthermore, the captured images undergo Sobel edge detection, a technique crucial for highlighting edges and extracting features like object boundaries. This process involves complex Verilog code to read data from SDRAM, perform Sobel edge detection, and extract text from the image. The extracted text is then compared with a known dataset of texts stored in the FPGA's memory to make a final decision regarding the IC's testing.

Additionally, the FPGA controls a servo motor to change the direction of a funnel, which classifies the ICs into their desired paths for segregation. Then, the system waits for the next IC to arrive, completing the segregation cycle. The FPGA plays a central role in the system, controlling various mechanical components and processing image data for efficient IC segregation. Our approach offers a reliable, efficient, and scalable solution for IC segregation, with potential applications in electronics manufacturing and testing industries.

2. Related Work

Deval Patel et al [1] concentrates on the image acquisition aspect of gesture recognition, showcasing the utilization of the OV7670 CMOS camera chip sensor connected to an FPGA DE-1 board. O.Vignesh et al [2] focuses to detect and extract words and letters efficiently using FPGA-based hardware architecture. Surbhi Chhabra et al [3] focuses on presenting an FPGA

algorithmic model for efficient license plate detection, comparing three approaches: Edge-based, Connected-Component-based, and Histogram-based. Adesh Kumar et al [4] concentrates on designing, modeling, and simulating a proposed method for text detection and extraction, leveraging the Haar DWT approach. Baby Sathya S et al [5] offers a promising approach to digitizing skewed document images, especially in historical and archival settings. S Navaneethan et al [6] aims to design and implement a video processing system using FPGA technology, with a focus on resource efficiency.

Cristinel Ababei et al [7] presents an open-source bare metal digital camera system implemented on an FPGA, specifically the DE2-115 board. The system is described in VHDL and tested on the FPGA chip. Afnan Alahmadi et al [8] aims to achieve robust real-time face detection using Field-Programmable Gate Arrays (FPGA) based on the Viola-Jones algorithm. Xiaokun Yang et al [9] introduces a scalable image/video processing platform implemented on a Field-Programmable Gate Array (FPGA). This platform is designed to capture images using an affordable OV7670 camera and display the original, in-process, and final image results in real-time on a VGA-interfaced monitor.

3. Proposed Work

The Figure 1 depicts the overall process of IC segregation.

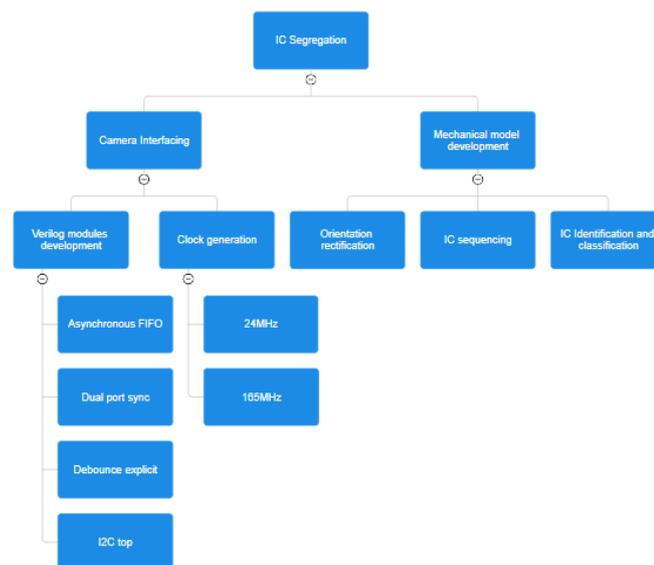


Figure 1. Overall Process of IC Segregation

3.1 IC Segregation

3.1.1 Orientation rectification

A vibrator like model is developed as a part of the mechanical model. The purpose of this part is to tilt the integrated circuits such that the top of the IC faces the ground as proper orientation is required to classify them. It uses a DC motor which facilitates the forward and backward motion of the shaker for producing the necessary vibrations.

3.1.2 IC Sequencing

The conveyor belt is used to deliver the mixed ICs one by one to the region where the camera captures the image of each IC. The conveyor belt is designed using the DC motor that rotates at 360 degrees. The DC motor is powered by the FPGA.

3.1.3 IC Identification using Image Processing

The ICs reach the dropper stand which is transparent. An OV7670 camera module is used to capture the image of the top surface of the IC. The camera is interfaced with the FPGA for further processing of the captured image. Altera DE1 FPGA board is used for image processing. The dropper stand is also controlled by a servo motor that rotates 180 degrees. For interfacing the OV7670 camera with Altera Cyclone II FPGA [10], Verilog code for modules like asynchronous FIFO, dual port sync, I2C master, debounce explicit were developed and simulated using Altera ModelSim software. The camera module operates at 24MHz and the SDRAM operates at 165MHz. Hence Qsys tool of the Altera Quartus II software has been used for the clock generation of the two frequencies.

Sobel edge detection is a technique used in image processing to highlight edges by calculating the gradient of the image intensity. It is significant for its ability to extract crucial features like object boundaries, aiding in tasks such as object detection and image segmentation [13]. Hence we use it to detect text from image.

The FPGA performs the image processing [11] with the help of the Verilog code that is developed. The purpose of the code is to read the data from the SDRAM and perform sobel edge detection [12] to detect the names of the respective ICs. The process of sobel edge detection involves arranging the image data into three arrays and traversing the sobel operators

across the arrays. Further, the convolution operation is performed by two sobel operators. Hence two gradients are obtained namely G_x and G_y which are then added to obtain the final gradient value G . The convolution process requires 9 pixel values which includes one target pixel and 8 neighbouring pixels. The sobel operators have 9 elements each. After the sobel edge detection, the data is again written into the memory of FPGA.

After performing sobel edge detection [14], the text is extracted from the image and compared with the known dataset of texts that are stored in the dedicated memory of DE1 FPGA to make the final decision for segregating the ICs. The final decision is provided by the FPGA.

3.1.4 IC Classification

The FPGA controls a servo motor that rotates at 180 degrees to change the direction of the funnel which classifies the ICs into their desired paths for segregation. Based on the decision made after the Sobel edge detection and text extraction [15], the FPGA controls the servo motor to turn in either of the two directions where the ICs will be collected separately for which a Verilog code has been developed which is executed after the text comparison process.

3.1.5 Waiting for Next IC

Once the IC is tested and the result is evaluated, the model waits until the next IC comes for segregation process.

4. Results and Discussion

The side view, front view and top view of the mechanical model has been shown in Figure 2, 3, and 4 respectively. It performs the necessary actions of orientation rectification, IC sequencing, and IC identification.

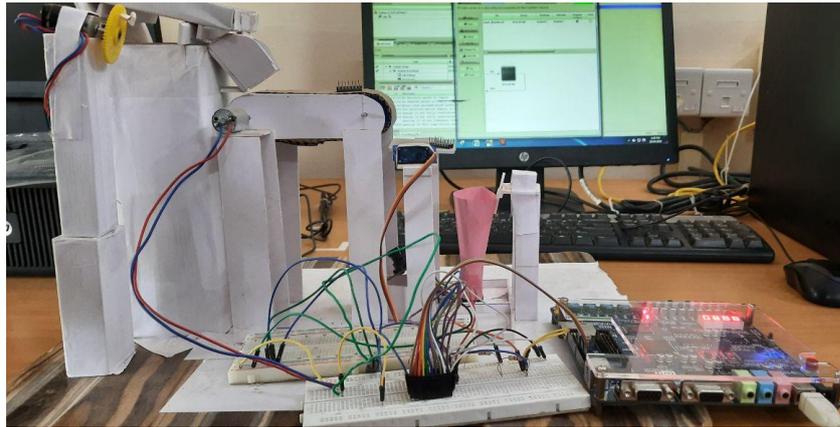


Figure 2. Side View of the Mechanical Model

The Figures 5 and 6 shows the results after the successful simulation of Sobel edge detection algorithm that is performed by the FPGA. The Figures 7, 8, 9, 10, and 11 shows the simulation results of the Verilog modules that were developed for interfacing the camera module with the FPGA. Figure 7 shows the simulation result of asynchronous FIFO module. Figure 8 shows the simulation result of debounce explicit module. Figure 9 shows the simulation result of clock generation using Qsys tool. Figure 10 shows the simulation result of I2C top module. Figure 11 shows the simulation result of dual sync port module.

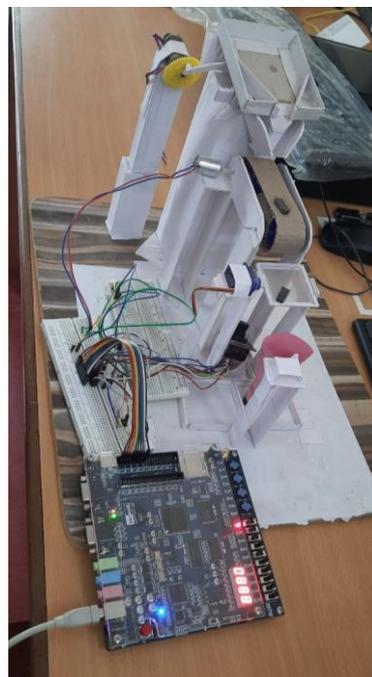


Figure 3. Front View of the Mechanical Model

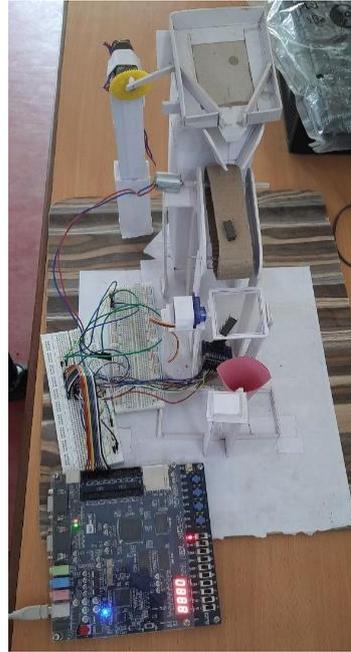


Figure 4. Top View of the Mechanical Model

Table 1. Components used in the Mechanical Model

S.No.	Component name	No. of components used
1	Servo motor	2
2	DC motor	2
3	Altera DE1 cyclone II FPGA board	1
4	OV7670 Camera module	1
5	Funnel	1
6	Transparent glass plate	1
7	Conveyor belt	1
8	Breadboard and connecting wires	1

The edge detection is performed successfully of an image using an online simulation tool called EDA playground and the output as decimal values and waveforms are attached in Figure 5 and 6 respectively. In Figure 6 G [0] is the least significant bit and for each clock pulse, edge detection is performed for subsequent target pixels. The first gradient value obtained is “101010” from the waveform output which is same as the decimal output “42”.

```
VCD info: dumpfile main.vcd opened for output.  
42  
58  
44  
66  
80  
82  
68  
74
```

Figure 5. Output of Simulation

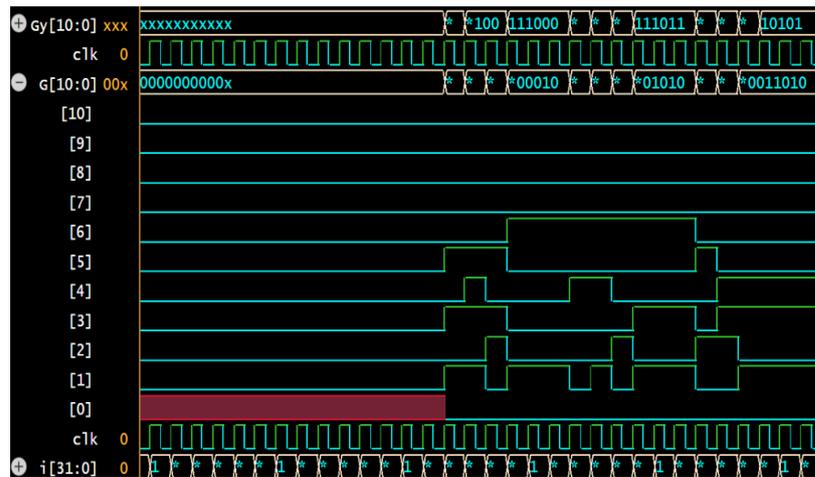


Figure 6. Output as Waveform

The asynchronous FIFO module implements an asynchronous FIFO (First-In-First-Out) buffer with dual-clock domain support. It allows data transfer between two clock domains that operate at different frequencies or have different phases, such as a camera interface at 24MHz and an SDRAM interface at 165MHz. In the Figure 7, once the write signal becomes high, data is written and read successfully.

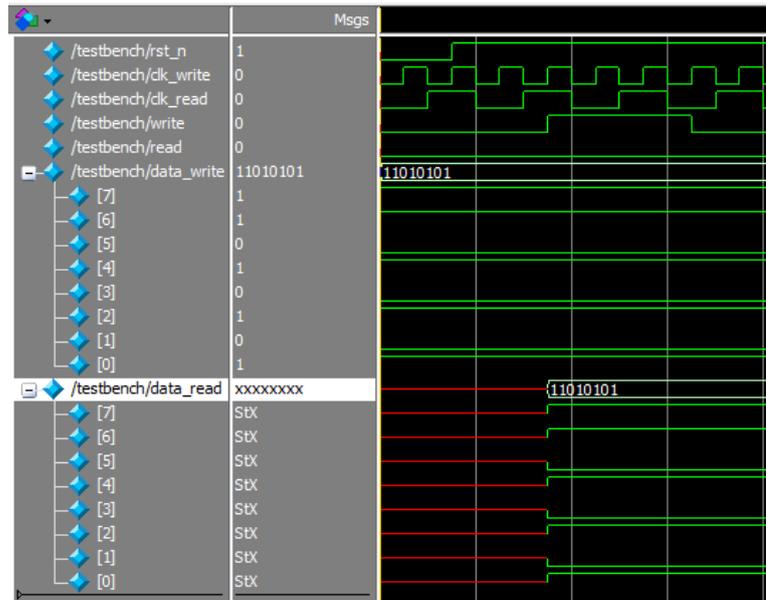


Figure 7. Asynchronous FIFO Module Simulation Output

The debounce explicit module implements a debounce circuit for a switch using a finite state machine (FSM) and a timer. The purpose of debouncing is to eliminate multiple transitions of the switch caused by mechanical contacts bouncing against each other when the switch is pressed or released. 4 switches are used for adjusting the brightness and contrast of the camera module. In the Figure 8, the db_level signal indicates the stable state of the switch and the db_tick signal indicates the valid transition of the switch.

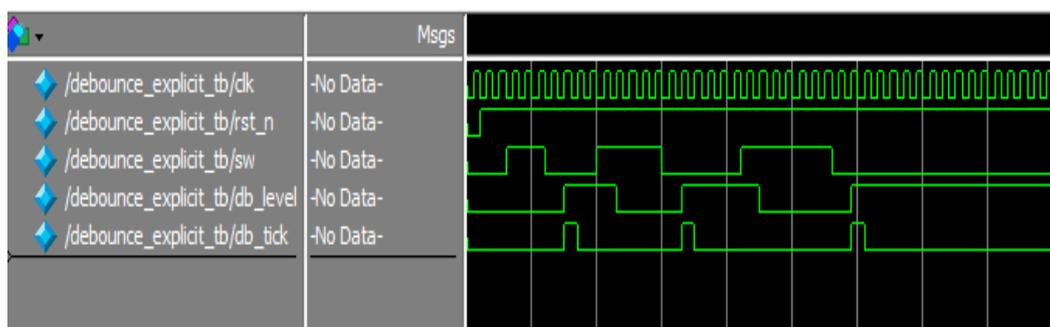


Figure 8. Debounce Explicit Module Simulation Output

Qsys software is used to generate clocks of two different frequencies for which two components namely the clock source and PLL has been used. The output of the clock source is given as input to the PLL. The output of the PLL will be the desired clock frequency.

Use	Connections	Name	Description	Export	Clock	Base
<input checked="" type="checkbox"/>		aitpll_0	Avalon ALTPLL			
		inclk_interface	Clock Input	Double-click to export	clk_0	
		inclk_interface_reset	Reset Input	Double-click to export	[inclk_interfa...]	
		pll_slave	Avalon Memory Mapped Slave	Double-click to export	[inclk_interfa...]	
		c0	Clock Output	aitpll_0_c0	aitpll_0_c0	
		areset_conduit	Conduit	Double-click to export		
		locked_conduit	Conduit	Double-click to export		
		phasedone_conduit	Conduit	Double-click to export		
<input checked="" type="checkbox"/>		clk_0	Clock Source			
		clk_in	Clock Input	clk		
		clk_in_reset	Reset Input	reset		
		clk	Clock Output	Double-click to export	clk_0	
		clk_reset	Reset Output	Double-click to export		

Figure 9. Clock Generation using Qsys Tool

The I2C master module implements a master for the I2C (Inter-Integrated Circuit) communication protocol. I2C is a widely used protocol for communication between integrated circuits, typically on a circuit board. Here it is used to write and read data into and from the SDRAM. In the Figure 10, start and stop conditions are provided and the data is written into the SDRAM by specifying the address of the location.

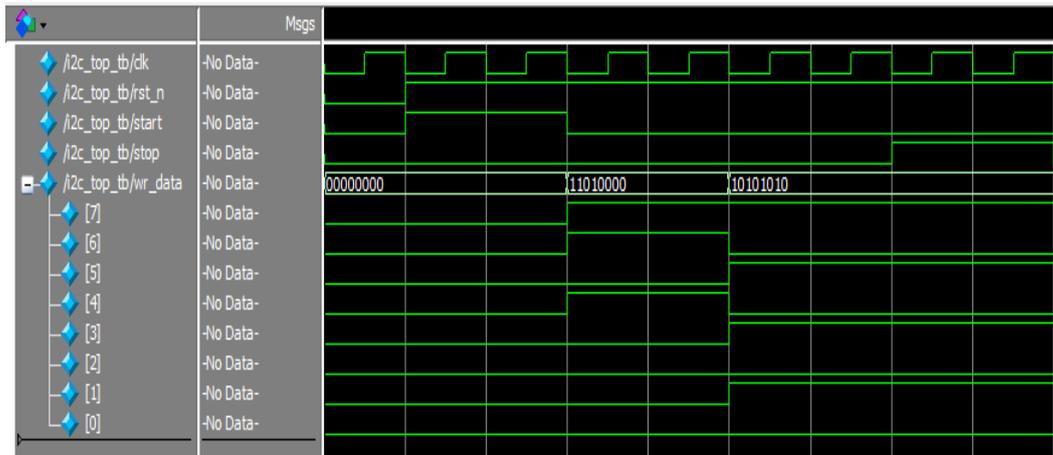


Figure 10. I2C Master Module Simulation Output

The dual port sync module provides a dual-port synchronous RAM, which allows simultaneous read and write operations from different clock domains. This is essential in the FIFO to enable writing data into the FIFO from one clock domain (the write clock domain) while reading data from another clock domain (the read clock domain).

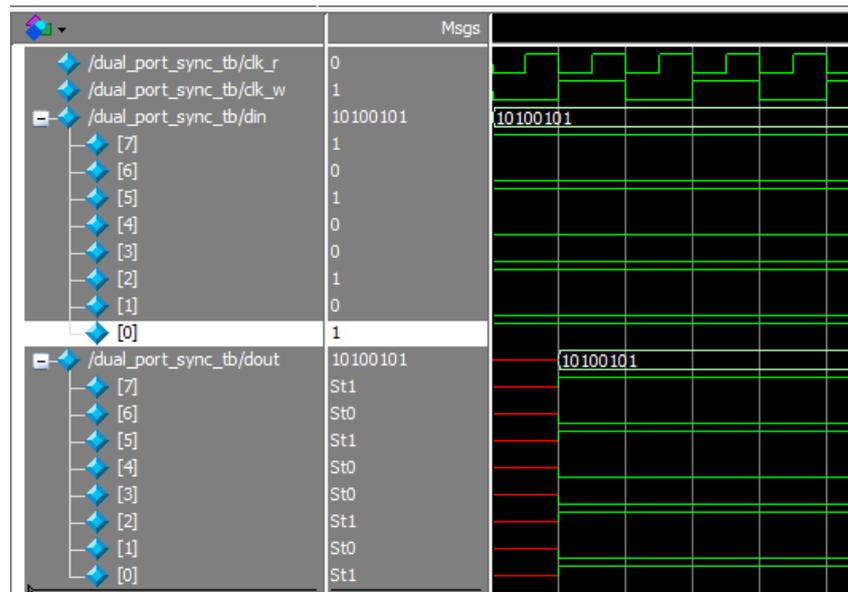


Figure 11. Dual Sync Port Module Simulation Output

The proposed model can be used for the application of IC segregation which is an important task especially in places like college laboratories and industries.

5. Conclusion

In conclusion, our FPGA-based system offers a comprehensive solution for the segregation of ICs, combining mechanical and digital components to automate the process. The system's ability to orient, sequence, identify, and classify ICs streamlines the segregation process, improving efficiency and accuracy. Future work could focus on enhancing the system's speed and scalability to accommodate larger volumes of ICs.

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