

Low Power and Delay Efficient 4x4 Array Multiplier Using 20T Hybrid Adder in 90nm Technology

Vishva Sakthi M¹, Sathiya Prakash B L², Srividyaabarathi A³

Department of Electronics and Communication Engineering, Government College of Technology,
Coimbatore, Tamil Nadu, India

E-mail: ¹alphavishva@gmail.com, ²sathiyaprakashbl2003@gmail.com, ³srividyaabarathi@gmail.com

Abstract

In this paper, the 4x4 array multiplier was designed and its power Delay Product (PDP) was analyzed. An array of full adders and half adders is used in an array multiplier, a combinational circuit, to multiply two binary values. The total power consumed by the array multiplier can be minimized by introducing a hybrid adder which constitutes 20T. In the 20T hybrid adder maximum power consumption is mostly dependent on the performance of the 10T XOR-XNOR circuit. As a result, it offers both full swing output and good capabilities without the need for an external inverter. Therefore, the array multiplier was designed by a hybrid adder instead of a conventional adder circuit to achieve low power and delay efficient multiplier circuit. The hybrid adder circuit outperforms its counterparts showing that PDP reduces 18% more than available conventional full adders. Using 90nm CMOS technology, the suggested circuits' performance is evaluated by stimulating them in a cadence virtuoso environment.

Keywords: Array Multiplier, 20T Hybrid Adder, 10T XORXNOR, Power Delay Product (PDP)

1. Introduction

The focus of VLSI techniques is greatly on the low power and delay-efficient circuits. Because more and more portable applications require small-area, low-power, high-throughput circuits [1-3].

In the realm of digital systems, efficient multiplication lies at the heart of various computational tasks, from signal processing to cryptography. With the pervasive integration of electronics into everyday life, the demand for energy-efficient designs has surged, particularly in mobile and battery-powered applications. In this context, minimizing power consumption and reducing delay in arithmetic operations are paramount objectives for optimizing the performance of digital systems. Among these operations, multiplication stands as a cornerstone, influencing the overall efficiency and speed of numerous algorithms and applications. Hence, the development of low-power, delay-efficient multiplication techniques holds immense significance for advancing the capabilities of modern electronic devices [4].

This paper introduces a novel approach to address this critical need: a low-power, delay-efficient array multiplier. By leveraging innovative design strategies and optimization techniques, this multiplier promises to offer significant improvements over traditional approaches in terms of both power consumption and delay [5-10].

The remainder of the paper is organized as follows: In section II, the modifications of hybrid adders are discussed and a 4x4 array multiplier using conventional adders and modified hybrid full adders are compared. Section III contains the results based on the comparisons. Section IV contains the conclusion of this paper.

2. Proposed Method

A. Proposed Hybrid Adder

1A. Conventional Full Adder

A traditional full adder is a combinational circuit with three inputs and two outputs: sum and carry. In CMOS technology, constructing a full adder requires 28 transistors. This large number of transistors leads to higher power



Figure 1. Conventional Full Adder (Deol, 2021)

consumption and increased delay. The sum output is derived from equation (1), while the carry output is determined by equation (2).

$$\text{SUM} = (A \oplus B) \oplus C'IN \tag{1}$$

$$\text{CARRY} = AB + BC'IN + AC'IN \tag{2}$$

2A. Proposed Hybrid Adder

The hybrid adder proposed is designed with three distinct modules to enhance performance and efficiency

- **Module 1:** This module features a 10-transistor XOR-XNOR circuit, which optimizes the logic operations and reduces power consumption
- **Module 2:** This module is dedicated to computing the sum output of the adder, ensuring accurate addition results.
- **Module 3:** This module manages the carry output of the adder, facilitating the correct propagation of carry bits.

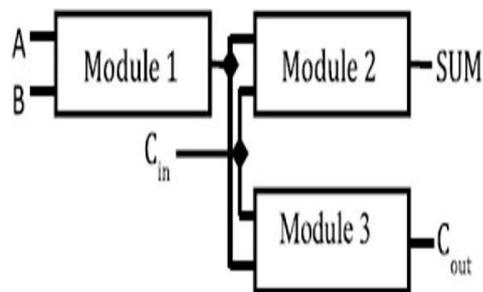


Figure 2. Block Diagram of Proposed Hybrid Adder (Jayaram, 2018)

i) Module 1:10T XOR-XNOR Circuit

The XOR-XNOR circuit can be built using two different methods. One method starts with designing the XOR circuit and then generating the XNOR output by adding an inverter. This approach is referred to as the Transmission Gate Adder (TGA). However, because the XOR and XNOR outputs are not generated simultaneously, this technique has a significant downside in that it can result in incorrect switching and glitches in the outputs of Module 2 (the sum circuit) and Module 3 (the carry circuit). The XOR-XNOR circuit is made to concurrently create both outputs in order to solve this issue. This design ensures synchronized operation and prevents glitches, resulting in more reliable performance.

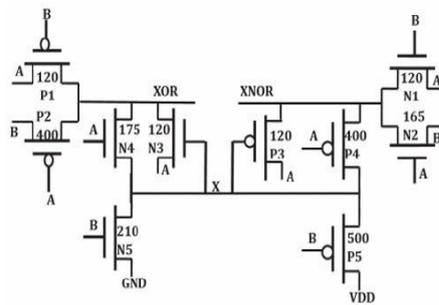


Figure 3. Module I 10T XOR-XNOR Circuit (Tejaswini M. L, 2021)

Based on Complementary Pass-Transistor Logic (CPL), ten transistors are used in this design to produce the XOR-XNOR circuit. The schematic view of the circuit is illustrated in the accompanying Figure 3. This approach ensures efficient operation and minimizes the number of transistors required.

Five of the ten transistors in this construction are utilized to produce the XOR circuit, while the remaining five are used to form the XNOR circuit. Two pMOS transistors (P1 and P2) and three nMOS transistors (N3, N4, and N5) make up the XOR circuit. On the other hand, three pMOS transistors (P3, P4, and P5) and two nMOS transistors (N1 and N2) make up the XNOR circuit. With this setup, full output swing XOR and XNOR outputs can be generated simultaneously. In the XOR circuit, N4 and N5 function as restoring transistors to guarantee a full-swing output, while N3 serves as a feedback transistor. P1 and P2 are connected in parallel as part of the Pass-Transistor Logic (PTL) architecture. Similar to this, P4 and P5 act as restoring transistors, P3 is a feedback transistor, and N1 and N2 are connected in parallel as PTL in the XNOR circuit. In the XNOR circuit, P4 and P5 act as restoring transistors, P3 is a

feedback transistor, and N1 and N2 are coupled in parallel as PTL. For greater clarity, the charging and discharging pathways for the XOR and XNOR outputs are displayed in the table.

Table 1. Path Flow for Various Input Combinations (Tejaswini M. L, 2021)

INPUTS (A, B)	XOR (Full Swing)	XOR (Partial Swing)	XNOR (Full Swing)	XNOR (Partial Swing)
00	N3	P1, P2	P4, P5	--
01	P2	--	N1	P4, P3
10	P1	N4, N3	N2	--
11	N4, N5	--	P3	N1, N2

- When A and B are set to 01, transistors P2, N1, and P4 are activated. This configuration allows logic "1" to be transmitted at the XOR output and logic "0" at the XNOR output.
- Transistors P1, N2, and N4 are turned on when A and B are set to 10 transistors, producing logic "1" at the XOR output and logic "0" at the XNOR output.
- For A and B as "00," transistors P1, P2, P4, and P5 are triggered, producing logic "0" at the XOR output and logic "1" at the XNOR output.
- Also, for A as well as B as "11," transistors N1, N2, N4, and N5 are triggered, resulting in logic "1" at output of XOR and logic "0" at output of XNOR.

The described circuit employs a Pass-Transistor Logic (PTL) configuration along with restoring transistors and feedback transistors to ensure proper functionality and full output swing for both XOR and XNOR outputs under various input conditions.

ii)Module 2: Sum Circuit

Module 2, functions as the sum circuit, and is realized using equation (3). The sum output of proposed hybrid full adder can be derived from the XNOR and the XOR module I output with the preceding carry, CIN. The equation (3) is expressed as:

$$\text{SUM} = (A \oplus B) \oplus C'IN + (A \oplus B)' \oplus C'IN \quad (3)$$

A CMOS-based implementation of module II is depicted in the Figure 4. The CMOS logic style is used in this sum circuit, which has N and P blocks at the bottom and top of the

circuit, respectively. It provides better delay performance and lower power consumption with just four transistors.

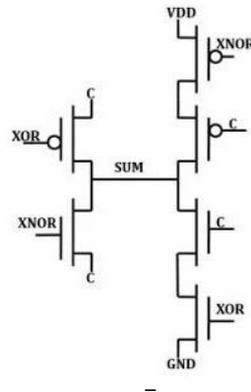


Figure 4. Module # Sum circuit (Tejaswini M. L, 2021)

iii) Module 3: Carry Circuit

Module 3, tasked with handling the carry, operates according to equation (4). By combining the XOR and XNOR outputs from Module 1 with the previous carry, CIN, as input signals, the carry output of the entire adder is calculated. The delay of Module 3 greatly affects the total delay in cascading systems since it depends on the carry output of the preceding full adder.

$$COUT = (A \oplus B) A + (A \oplus B) CIN \tag{4}$$

The CMOS-based implementation of module III, depicted in the Figure 5, utilizes four transistors. This design not only minimizes power consumption but also enhances delay performance compared to conventional approaches.

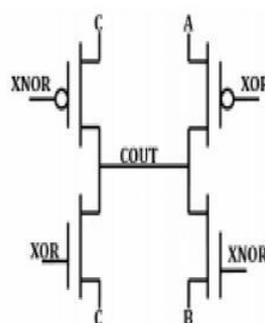


Figure 5. Module III – Carry circuit (Tejaswini M. L, 2021)

B. Proposed Array Multiplier

1B. Conventional Array multiplier

Utilized in digital computation, an array multiplier facilitates the multiplication of binary numbers. Its operation involves a collection of full and half adders arranged in an array, enabling the simultaneous addition of multiple product terms. Before reaching the array of adder, an AND gate array is utilized to produce the several product terms. Structurally, the array multiplier demonstrates regularity and operates according to the add-shift algorithm principle. In an array multiplier, each bit of the multiplier is sequentially multiplied by each bit of the multiplicand, producing partial products. These partial products are added together to generate the final product. The regular design structure of the array multiplier allows for efficient parallel processing of the partial products, leading to faster multiplication compared to sequential methods. Additionally, the add-shift algorithm principle employed by the array multiplier optimizes its performance by minimizing reducing the number of operations essential to compute the final result. Overall, array multipliers are widely used in digital arithmetic circuits due to their efficiency and scalability.

$$\text{Partial product} = \text{Multiplicand bit} * \text{Multiplier bit} \quad (5)$$

The formation of partial products in an array multiplier is governed by equation (5), where each bit of the multiplicand is multiplied by each bit of the multiplier. This process involves utilizing AND gates for product generation, with summation accomplished through a combination of full adders and half adders. The partial products are then shifted according to their respective bit orders. In an n array multiplier, the computation of partial products involves employing n AND gates. The addition of these partial products is executed using n*(n-2) full adders and n half adders. The multiplication of a 4-bit binary number is illustrated in the provided figure, where a₀, a₁, a₂, and a₃ represent the multiplicand, and b₀, b₁, b₂, and b₃ denote the multiplier. The summation of all products yields the partial products, and the cumulative sum of these partial products represents the final product.

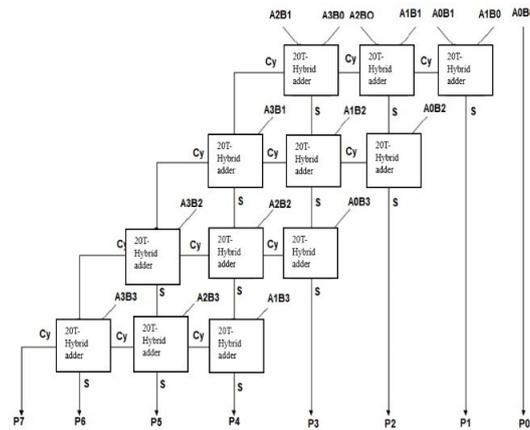


Figure 8. Block Diagram of Array Multiplier using 20T Hybrid Adder

3. Result Analysis

Schematics for the conventional full adder, 20T hybrid adder, conventional array multiplier, and modified array multiplier were meticulously crafted and subjected to rigorous performance analysis within the Cadence Virtuoso platform, utilizing the 90nm technology node. This comprehensive evaluation allowed for a detailed comparison of their respective efficiencies, power consumption, and delay characteristics, enabling informed design decisions for future implementations. The schematic view and the simulation result are observed in Figure 9-20

A. Schematic View

1A. Conventional Full Adder

The conventional full adder circuit is constructed using CMOS logic, employing a total of 28 transistors. The sum and carry circuits are meticulously designed using CMOS logic principles. Symbols are crafted to represent the various components and connections within the full adder circuit, facilitating its design and implementation. This approach ensures the efficient and reliable operation of the conventional full adder within the overall digital system.

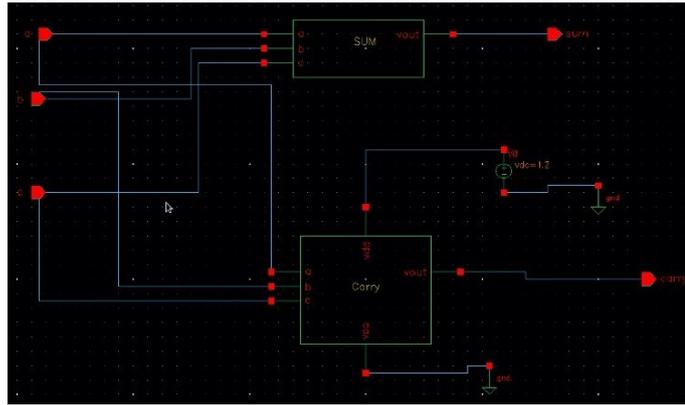


Figure 9. Schematic View of Full Adder

2A. 20T Hybrid Adder

The hybrid adder was meticulously crafted utilizing a 20-transistor (20T) configuration. Within this design, the sum and carry circuits were ingeniously engineered using CMOS logic principles, ensuring efficient operation and low power consumption. Additionally, the “XOR-XNOR” circuit, crucial for generating inputs to the sum and carry circuits, was thoughtfully designed using CPL (Complementary Pass-Transistor Logic) logic, enhancing the adder's performance and versatility. This strategic combination of CMOS and CPL logic ensures the hybrid adder's reliability and effectiveness in various digital applications.

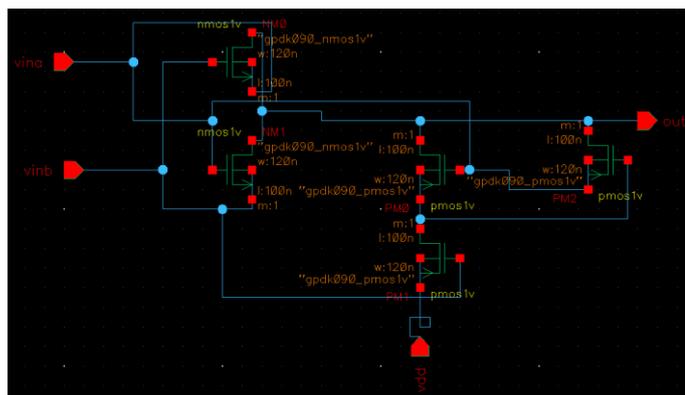


Figure 10. Schematic View of XNOR Circuit

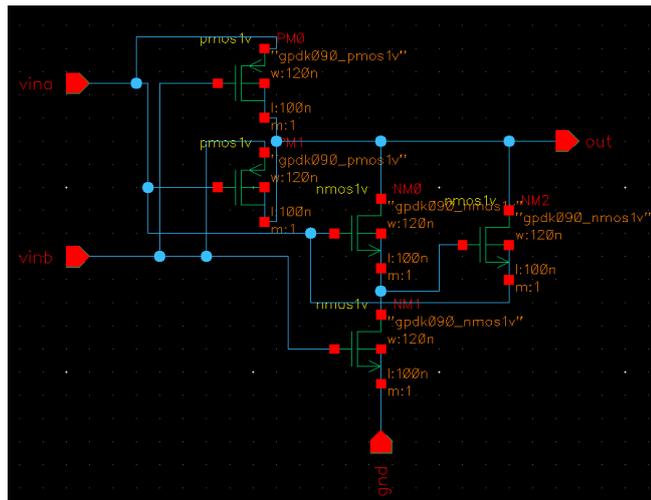


Figure 11. Schematic View of XOR Circuit

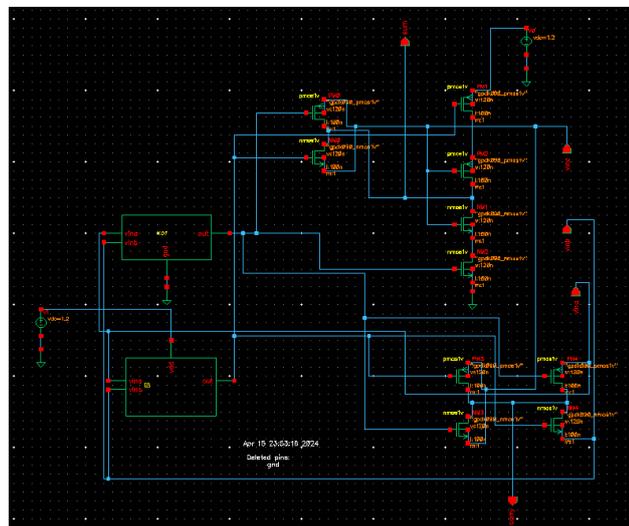


Figure 12. Schematic View of 20T Hybrid Adder

3A. Conventional Array Multiplier

To construct the partial product, AND gates are engineered utilizing CMOS logic principles. The conventional full adders, along with these CMOS-based AND gates, are integrated to formulate the conventional array multiplier. This meticulous combination ensures the efficient computation of partial products within the array multiplier, facilitating accurate multiplication operations in digital circuits.

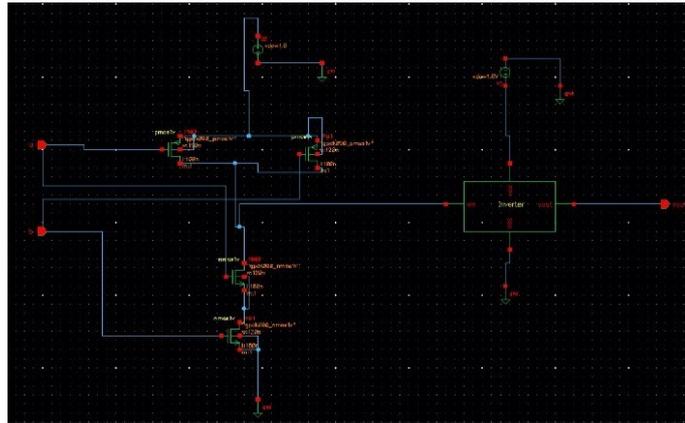


Figure 13. Schematic View of AND Gate

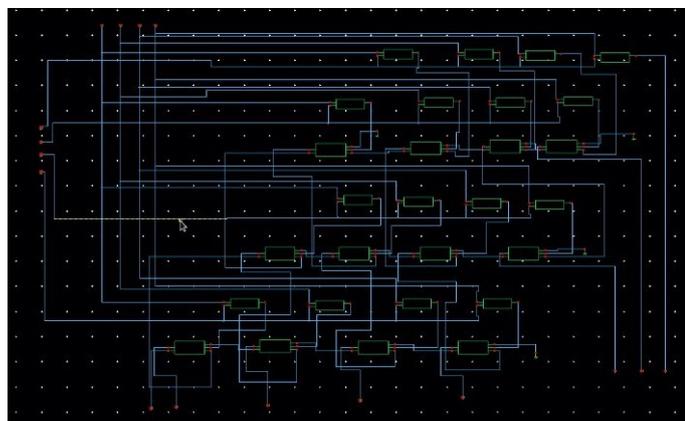


Figure 14. Schematic View of Conventional Array Multiplier

4A. Array Multiplier Using 20T Hybrid Adder

To improve the efficiency of the array multiplier circuit in terms of both delay and power consumption, the traditional full adder is substituted with the 20-transistor (20T) hybrid adder. This replacement is aimed at optimizing the performance of the array multiplier, ensuring that it meets the stringent requirements of modern digital systems while minimizing power consumption and reducing delays.

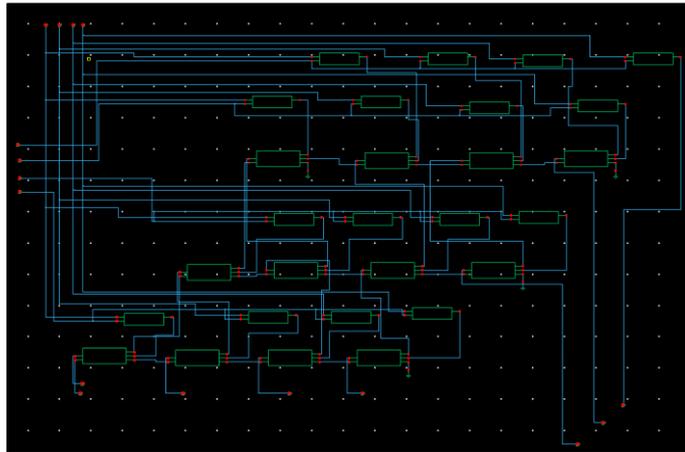


Figure 15. Schematic View of Array Multiplier using 20T Hybrid Adder

B. Output Waveforms

The transient response and the average power were plotted in the graph.

1B. Conventional Full Adder

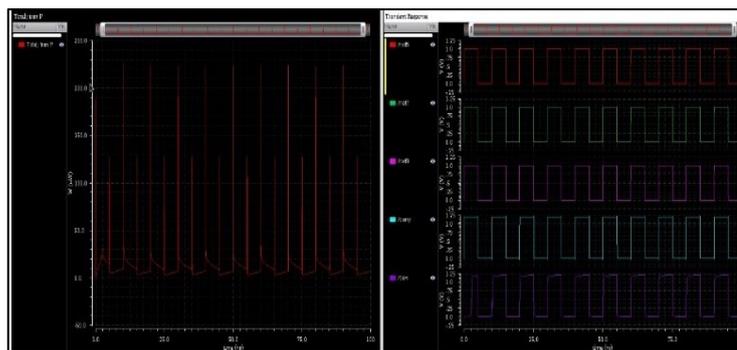


Figure 16. Transient Response and Power of Conventional Full Adder

2B. 20T Hybrid Adder

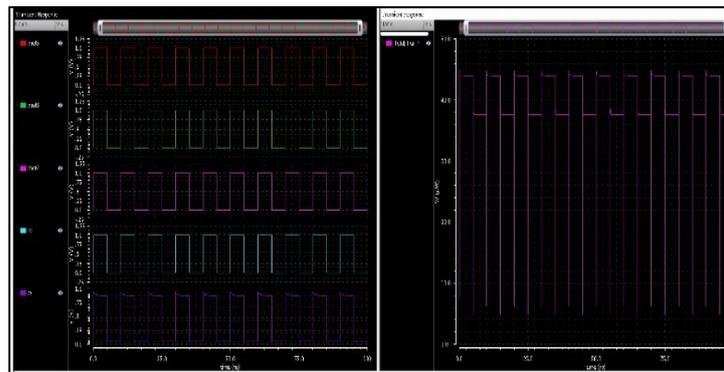


Figure 17. Transient Response and Power of 20T Hybrid Adder

3B. Conventional Array Multiplier

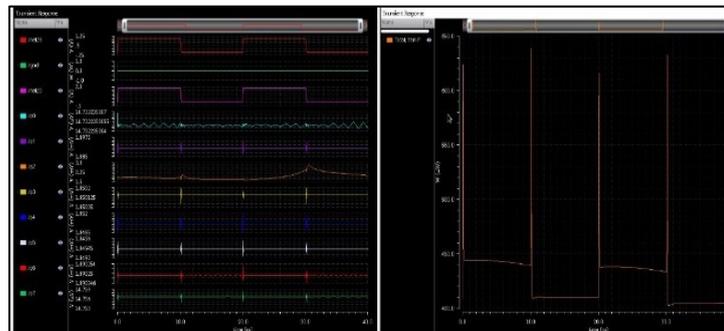


Figure 18. Transient Response and Power of Conventional Array Multiplier

4B. Array Multiplier Using 20T Hybrid Adder

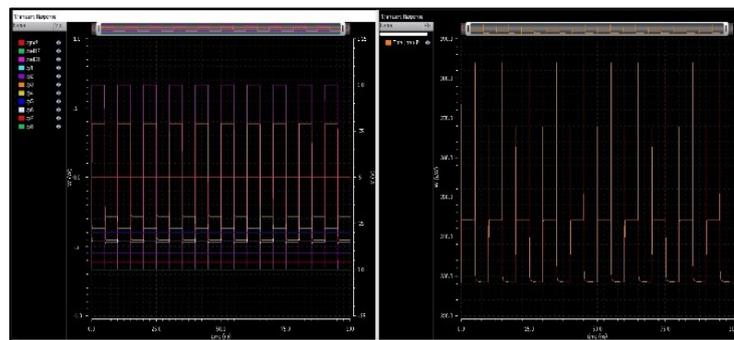


Figure 19. Transient Response and power of Array Multiplier using 20T Hybrid Adder

Power & Delay Analysis

The parameters PDP, delay and average power of the conventional adder, 20T Hybrid Adder, Conventional Array Multiplier, and Array Multiplier using 20T Hybrid Adder are tabulated and comparison was done using a bar chart.

Table 2. Performance Analysis

Parameter	Average Power (μ W)	Delay (ns)	PDP (pJs)
Conventional Full adder	129.4	4.8137	0.6228
20T hybrid Adder	40.55	2.8439	0.1153
Conventional Array Multiplier	513.9	47.1455	24.228
Array Multiplier Using 20T hybrid Adder	343.8	41.1126	14.134

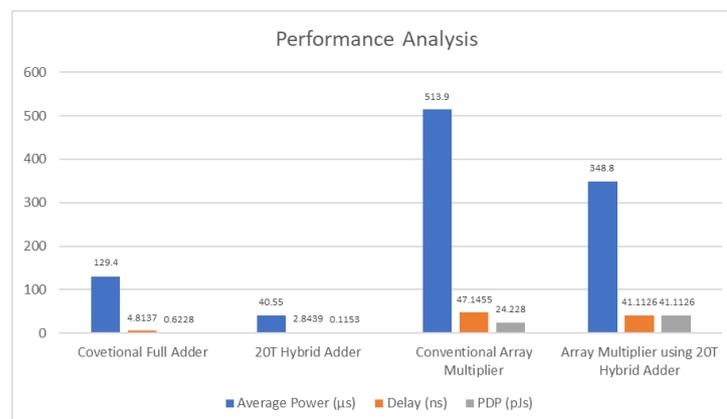


Figure 20. Comparison of Parameters using Bar Chart

4. Conclusion and Future Enhancement

Using a 20T Hybrid adder we designed a 4x4 Array, Multiplier and its power delay product (PDP) were analyzed. It achieves 18% of PDP reduction than the conventional adder circuit and the area will be reduced. In the future, multilevel circuits could be achieved and we use this Array Multiplier in image processing, filter design, MAC unit, and ALU by combining these techniques to further enhance performance.

References

- [1] Tejaswini M. L, Aishwarya H, Akhila M, B. G. Manasa-"High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR–XNOR Cell, International Journal of Advanced Research in Science, Communication and Technology (IJARSCT) Volume 8, Issue 1, August 2021. 263 -269
- [2] Naseri, Hamed, and Somayeh Timarchi. "Low-power and fast full adder by exploring new XOR and XNOR gates." *IEEE transactions on very large scale integration (VLSI) systems* 26, no. 8 (2018): 1481-1493.
- [3] M. A. Valazani and S. Mirzakhani, "A Novel fast, low power and high- performance XOR-XNOR cell", *IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 694–697.
- [4] C.-H. Chang, J. Gu, and M. Zhang, "A review of 0.18- μm full adder performances for tree-structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.
- [5] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *IEEE Proc.-Circuits, Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.
- [6] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, and A. Dandapat, "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit," *IEEE Trans. Very Large-Scale Integer. (VLSI) Syst.*, vol. 23, no. 10, pp. 2001–2008, Oct. 2015.
- [7] Amini-Valashani, Majid, Mehdi Ayat, and Sattar Mirzakuchaki. "Design and analysis of a novel low-power and energy-efficient 18T hybrid full adder." *Microelectronics journal* 74 (2018): 49-59.

- [8] Hasan, Mehedi, Md Shahbaz Hussain, Mainul Hossain, Mohd Hasan, Hasan U. Zaman, and Sharnali Islam. "A high-speed and scalable XOR-XNOR-based hybrid full adder design." *Computers & Electrical Engineering* 93 (2021): 107200.
- [9] Bui, Hung Tien, Yuke Wang, and Yingtao Jiang. "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates." *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 49, no. 1 (2002): 25-30.
- [10] Lin, Jin-Fa, Yin-Tsung Hwang, Ming-Hwa Sheu, and Cheng-Che Ho. "A novel high-speed and energy efficient 10-transistor full adder design." *IEEE Transactions on Circuits and Systems I: Regular Papers* 54, no. 5 (2007): 1050-1059.