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Fault-Resilient Brent-Kung Adder Design Using Advanced Built-in Self-Test (BIST) Architecture

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Abstract

In modern digital systems, ensuring both high performance and reliability is essential, especially in fault-sensitive environments. This research introduces the design and implementation of a fault-tolerant Brent-Kung adder, integrated with an advanced Built-In Self-Test (BIST) framework. The Brent-Kung adder, known for its efficient carry propagation and speed optimization, is augmented with BIST techniques to enhance its reliability and testability in digital systems. A Linear Feedback Shift Register (LFSR) is used to produce pseudo-random test patterns, while a Multiple Input Signature Register (MISR) compresses the adder's output into a compact signature for fault detection. The design is carried out in Verilog and synthesized using Xilinx Vivado 2019.1 to evaluate performance metrics, including area utilization, speed, and fault coverage. By combining the Brent-Kung adder's high-speed characteristics with a robust BIST framework, the research achieves an effective balance between performance and fault detection. This approach provides a promising solution for applications that require both computational efficiency and increased reliability in fault-sensitive environments.

Keywords: Brent-Kung Adder, Fault Resilience, Built-In Self-Test (BIST), Linear Feedback Shift Register (LFSR), Multiple Input Signature Register (MISR), and Fault Detection

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1. Introduction

In digital circuit design, adders play a important role as fundamental building blocks for various arithmetic operations. Among the different types of adders, the Brent-Kung adder has significant attention due to its logarithmic depth and reduced fan-out, making it efficient in both speed and hardware resources. However, in mission-critical applications, reliability and fault tolerance become paramount concerns. This drives the need for designing fault-resilient architectures that can sustain performance even in the presence of faults, which are increasingly common in modern high-density integrated circuits. As technology scales, transient faults caused by radiation, power glitches, and other environmental factors can lead to failures that compromise the functionality of such systems.

To address these challenges, fault detection and correction mechanisms have been integrated into adder designs, with Built-In Self-Test (BIST) architectures emerging as a prominent solution. BIST provides the ability for circuits to test themselves without requiring external testing equipment, significantly improving the fault coverage and operational autonomy of the system. The combination of the Brent-Kung adder's efficiency and an advanced BIST architecture offers a compelling solution to the challenge of maintaining high performance while ensuring robust fault resilience. The motivation behind this research is to explore and design a fault-resilient Brent-Kung adder that utilizes an optimized BIST structure for real-time fault detection and correction.

In this research, we focus on enhancing the Brent-Kung adder by incorporating advanced BIST techniques, which ensure continuous monitoring and testing of the adder's functional integrity. The proposed design focuses on detecting faults effectively and correcting them in real-time, reducing downtime and enhancing the system's overall reliability. Moreover, this work will contribute to the field of error-resilient computing by demonstrating how the integration of fault-tolerant methodologies in critical arithmetic units can enhance system longevity and robustness.

The organization of the proposed study is as follows: Section 2 provides a comprehensive review of the related work. Section 3 discusses the Advanced Bist Architecture for Fault Detection in Brent Kung Adder. Section 4 presents the Proposed Methodology, explaining the modifications made to the traditional architecture. Section 5 includes Simulation results, highlighting the performance and fault-resilience of the design. Finally, Section 6 Concludes the paper, discussing the findings and Section 7 explains potential future enhancements.

2. Related Works

N. Udaya Kumar et al. [1] presented the implementation and comparison of VLSI architectures for a 16-bit Carry Select Adder (CSLA) that utilizes a Brent-Kung adder in this research. The CSLA is an essential component for executing arithmetic operations. The study examines various VLSI architectures of the CSLA that incorporate the Brent-Kung adder. Experiments and simulations were conducted using XILINX 12.2. The findings reveal that the 16-bit CSLA with a Brent-Kung adder occupies less chip area, although it results in a slight increase in delay. Nevertheless, it demonstrates greater efficiency as a high-speed adder compared to other CSLA designs.

Aruru Sai Kumar et al. [2] presented a high-speed 8-bit Vedic multiplier design that utilizes Brent-Kung adders. Vedic mathematics streamlines complex calculations, facilitating easier mental computation. The multiplication algorithm employed, Urdhva Triyambakam, is favored over other methods because it can handle N x N bit numbers while minimizing latency. The architecture of the 8-bit Vedic multiplier consists of four 4-bit Vedic multipliers, two 8-bit Brent-Kung adders, one 4-bit Brent-Kung adder, and an OR gate. These 4-bit Vedic multipliers work together to form the 8-bit multiplier. The design is implemented in Verilog HDL and simulated and synthesized using Xilinx Vivado software. The proposed Vedic multiplier exhibits superior speed performance when compared to similar designs.

Ahmad Menbar et al. [3] proposed a concurrent Built-In Self-Test (BIST) architecture for combinational logic circuits. BIST allows hardware/software systems to conduct self-testing and is typically classified into offline and online techniques. This research introduces an innovative concurrent BIST method based on a duplication design. Instead of utilizing a conventional deterministic test pattern generation (TPG) algorithm, this approach uses a pre-computed test set chosen through a new methodology. Two Linear Feedback Shift Registers (LFSRs) are employed to generate the necessary test patterns, reducing the complexity and power consumption seen in traditional pattern detectors. Consequently, the design achieves a 43.9% reduction in area overhead compared to previous methods. Additionally, this technique employs a reduced version of the Circuit Under Test (CUT) as the golden reference circuit, rather than a full duplication design. However, it's important to note that this approach does not cover certain single stuck-at faults.

William T. Hale et al. [4] introduced a Built-In Test (BIT) design aimed at improving the detection and isolation of faults to boost system reliability. Their approach emphasizes self-diagnosis and fault isolation, particularly during aircraft ground maintenance, where there are fewer operational constraints, allowing for more flexibility in system input. This flexibility helps create optimal tests that enhance fault detection and isolation for both operators and maintenance personnel. The study outlines a general mathematical framework for developing built-in tests using a model-based active fault detection and isolation technique. A case study is presented to illustrate the difficulties in identifying and isolating faults under different conditions, demonstrating how system states contribute to these challenges. The proposed framework proves to be effective in designing built-in tests that can detect and isolate several common faults in aircraft environmental control systems. The authors conclude by emphasizing the method's value as a solution to a constrained optimization problem, where manipulating system inputs improves fault detection and isolation capabilities.

Ananthakrishnan et al. [5] conducted an FPGA-based study comparing the performance of various basic adder architectures with parallel processing adders. Adders play a critical role in nearly all modern integrated circuits. In the current era of digitalization, where miniaturization is a primary focus, achieving an optimal balance between area, power consumption, and delay is essential. Given their widespread use in complex digital circuits, enhancing adder performance can greatly accelerate binary operations. One key challenge in binary adders is the delay introduced by carry propagation. This study compares multiple adder architectures, such as the Carry Select Adder, Carry Lookahead Adder, Carry Increment Adder, Ripple Carry Adder, and Brent-Kung Adder. The comparisons were carried out using Hardware Description Language (HDL) on the Xilinx ISE 14.7 platform. Advanced bist architecture for fault detection in brent kung adder.

3. Advanced BIST Architecture for Fault Detection in Brent Kung Adder

A. BIST Architecture in Brent-Kung Adder

BIST architecture in a Brent-Kung Adder[7] is designed to enhance fault detection without the need for external testing hardware. The BIST system integrates two key components: the Linear Feedback Shift Register (LFSR) and the Multiple Input Signature Register (MISR). The LFSR generates a set of random like test patterns, which are applied as inputs to the Brent-Kung Adder. The adder processes these inputs and generates corresponding outputs. These outputs are fed into the MISR, which compresses the response into a signature. The signature is then compared with a predefined "golden signature," representing the correct response of a fault-free adder.

The LFSR operates based on a characteristic polynomial, typically of the form:

$$\mathrm{P(x) = xn + xk + 1}$$

where n and k define the taps for feedback in the LFSR. The MISR follows a similar polynomial structure for compressing the adder's output, ensuring efficient fault detection.

This BIST architecture[8] significantly reduces the need for external testing and provides real-time fault detection, making the Brent-Kung Adder more resilient. Figure 1 explains this architecture for fault detection in a Brent-Kung Adder, integrating key components like the LFSR, MISR and a Comparator. The LFSR generates random-like test patterns that are used for the Brent-Kung Adder, simulating various input scenarios. The adder's output is then fed into the MISR, which compresses the results into a unique signature representing the adder's behavior.

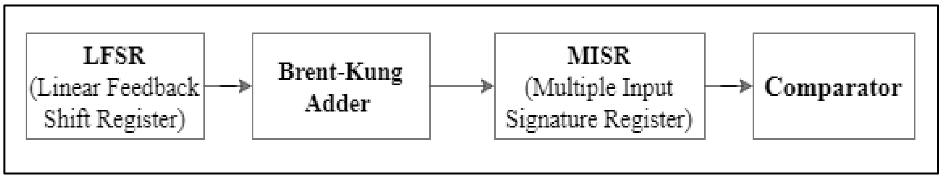

Figure 1. Block Diagram of the BIST Architecture

B. Design of Linear Feedback Shift Register (LFSR)

The Linear Feedback Shift Register [6] plays a vital role in the BIST architecture by generating random-like test patterns that are used for the Brent-Kung Adder for fault detection. As shown in the Figure.2, an LFSR is a type of shift register where the input bit is generated from a linear function of its previous state. A feedback loop is created using XOR gates, applying a characteristic polynomial to choose the taps, which guarantees the generation of a maximal-length sequence of test patterns. The generated patterns are fed into the Brent-Kung Adder, simulating various input conditions and testing its resilience to faults.

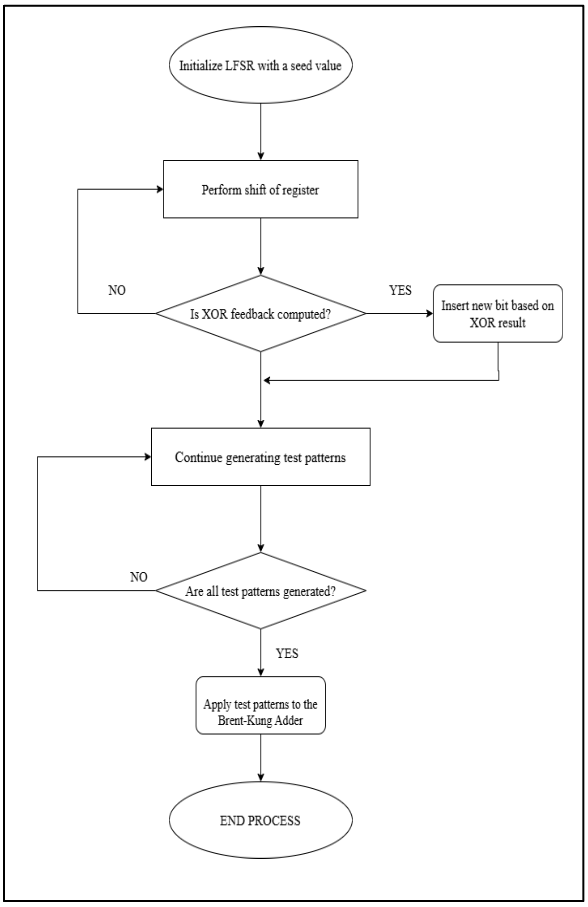

Figure 2. LFSR Process Flowchart for BIST Architecture

C. Design of Multiple Input Signature Register (MISR)

In the Fault-Resilient Brent-Kung adder design using advanced built-in self-test (BIST) architecture, the Multiple Input Signature Register (MISR) plays a vital role in compressing the output from the adder into a unique signature. The MISR is responsible for detecting any deviations from expected outputs, indicating faults in the Brent-Kung Adder. As shown in the Figure.3 MISR collects the outputs of the adder for each test pattern produced by the LFSR (Linear Feedback Shift Register). Using feedback from multiple XOR gates, it combines the outputs and stores a compressed result called a signature. This signature is evaluated against a precomputed golden signature representing the expected output for a fault-free adder. If the signatures mismatch, a fault is detected.

The characteristic polynomial of the MISR, similar to the LFSR, dictates the feedback structure. The polynomial ensures the MISR efficiently compresses multiple inputs while detecting faults. MISRs are widely used because they can significantly reduce the amount of data needed to check for faults, allowing for efficient fault detection without needing to store all outputs.

D. Test Flow in BIST Architecture

In the Fault-Resilient Brent-Kung adder design, the BIST architecture plays an vital role in testing the adder’s functionality, identifying faults, and improving system reliability. The test flow in BIST consists of three main stages: test pattern generation, response evaluation, and fault detection.

The test flow in the BIST architecture for the Fault-Resilient Brent-Kung Adder begins with test pattern generation by the Linear Feedback Shift Register (LFSR). The LFSR [14] generates random-like test patterns that simulate various input conditions, ensuring thorough testing of the adder’s performance. These test patterns are continuously applied as inputs to the Brent-Kung Adder.

The Brent-Kung Adder performs the necessary addition operations using the generated test patterns. The outputs produced by the adder [11] are passed on to the next stage of the BIST architecture to evaluate whether the adder has performed the calculations correctly.

The adder’s outputs are then processed by the Multiple Input Signature Register (MISR)[15] , which compresses the results into a compact signature using XOR feedback. This signature represents the adder's response to all applied test patterns, reducing the amount of data that needs to be stored or analyzed.

The generated signature is compared to a precomputed golden signature by a Comparator. The golden signature represents the correct output of a fault-free adder. If the signature generated by the MISR matches the golden signature, the adder is functioning as expected. If there is a mismatch, a fault is detected, indicating that the adder has produced incorrect results for the applied test patterns. This fault detection process ensures the accuracy and reliability of the Brent-Kung Adder.

E. Fault Detection Mechanism Using BIST

The fault detection [12] mechanism using Built-In Self-Test (BIST) in the Fault-Resilient Brent-Kung Adder is a systematic approach designed to identify and isolate faults within the adder's circuitry. This mechanism relies on the integration of test pattern generation, response evaluation, and comparison processes, enabling real-time assessment of the adder's performance.

The process begins with the Linear Feedback Shift Register (LFSR), which generates a series of random-like test patterns. These patterns are fed into the Brent-Kung Adder, simulating a wide range of input conditions. As the adder processes these inputs, it produces outputs that represent the results of the addition operations.

Once the outputs are generated, they are sent to the Multiple Input Signature Register (MISR). The MISR compresses these outputs into a compact signature using XOR feedback, significantly reducing the volume of data that needs to be evaluated. This signature encapsulates the adder’s behavior in response to the test patterns.

The final step in the fault detection mechanism [13] involves comparing the generated signature from the MISR with a precomputed golden signature, which represents the expected output of a fault-free adder. This comparison is conducted by the Comparator. If the generated signature matches the golden signature, the adder is deemed fault-free. Conversely, if there is a discrepancy, a fault is detected, indicating that the adder has produced incorrect results.

The BIST-based fault detection mechanism increases the reliability of the Brent-Kung Adder by quickly identifying and addressing any faults, thereby enhancing the system’s overall performance and robustness.

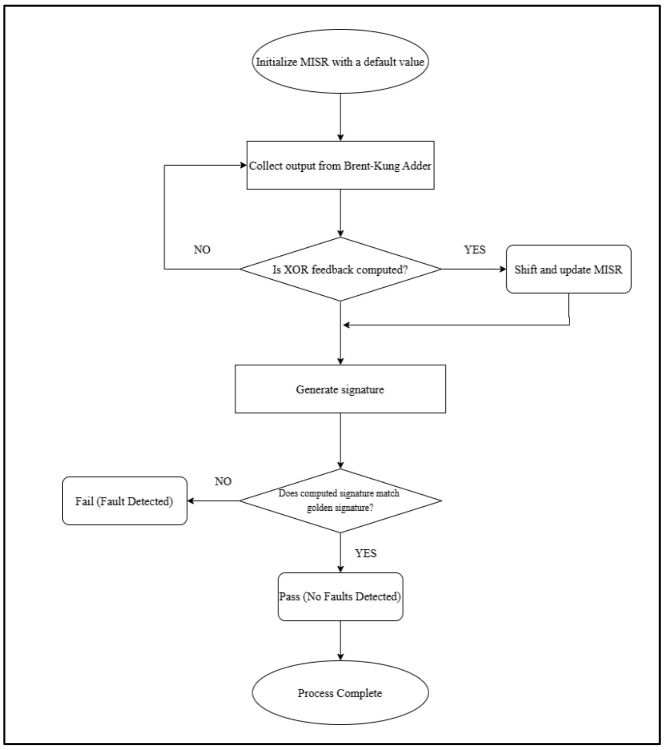

Figure 3. MISR Process Flowchart for BIST Architecture

4. Proposed Methodology

The methodology proposed for developing a fault-tolerant Brent-Kung adder with an advanced BIST architecture follows a structured approach to improve the reliability and performance of digital circuits. The Brent-Kung adder[10], a parallel prefix adder, is well-known for its efficiency in binary addition, especially in minimizing critical path delays compared to conventional adders. The methodology begins with a comprehensive literature review on the principles of Brent-Kung adder design and BIST techniques, providing a solid theoretical foundation for the study. This phase involves studying various architectures and their performance metrics to identify best practices and potential areas for innovation.

Following the literature review, the design phase commences with the realization of the Brent-Kung adder in Verilog. The design focuses on creating a modular and scalable architecture (Figure.4) [3] capable of handling multiple bits while ensuring minimal area usage and optimal speed. The adder's internal structure will use the hierarchical organization of carry computation, which reduces the number of logic gates required for operation. Simulation in Vivado will be conducted to verify the functionality of the Brent-Kung adder, ensuring that it performs correctly under various input conditions. Performance metrics such as delay, area, and power consumption will be carefully analyzed during this phase to validate the design's effectiveness.

Simultaneously, the advanced BIST architecture will be developed to enhance the fault detection capabilities of the Brent-Kung adder. The BIST methodology incorporates a pattern generator, specifically a LFSR, to produce test patterns applied to the adder inputs. The LFSR is designed to generate a pseudorandom sequence of patterns that thoroughly exercise the adder's logic, allowing for comprehensive testing of various fault conditions. Additionally, a Multiple Input Signature Register (MISR) will be integrated into the design to analyze the output of the adder. The MISR accumulates the outputs over time, generating a signature that can be compared against expected results to identify faults effectively.

The integration phase will involve embedding the BIST components within the Brent-Kung adder design. The BIST controller will manage the testing process, coordinating between the LFSR [9] and the MISR to automate the testing of the adder's functionality. During testing, the controller will activate the LFSR to generate input patterns and subsequently capture the adder’s output through the MISR. This automated testing process is crucial in ensuring that any potential faults, such as stuck-at faults or transient errors, are detected promptly and accurately. The performance impact of the BIST [4] on the overall design will also be evaluated, ensuring that the adder remains efficient while providing robust fault detection capabilities. The Brent-Kung adder employs a prefix tree to calculate the carry bits. The carry bits can be defined recursively:

$$\mathrm{Ck} = \mathrm{Gk} + \mathrm{Pk} \cdot \mathrm{Ck} - 1$$

Optimization efforts will be focused on refining the design to minimize area overhead and power consumption associated with the BIST architecture. Techniques for enhancing fault coverage and improving the resiliency of the design will be explored, ensuring that the final product meets the stringent requirements of modern digital circuits.

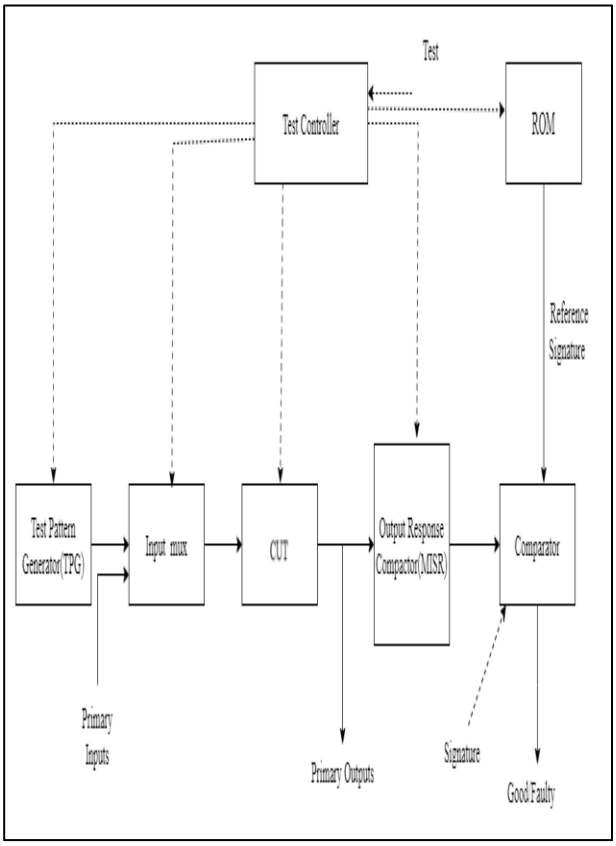

Figure 4. BIST Architecture [3]

Documentation of all design decisions, simulations, and performance metrics will be maintained throughout the study, aiding in the preparation of a comprehensive final report and presentation that showcases the innovative aspects of the fault-resilient Brent-Kung adder design utilizing advanced BIST techniques.

The BIST architecture for the Brent-Kung Adder integrates LFSR-based test pattern generation and MISR-based signature analysis to detect faults efficiently implies Overall Architecture (Figure.5).

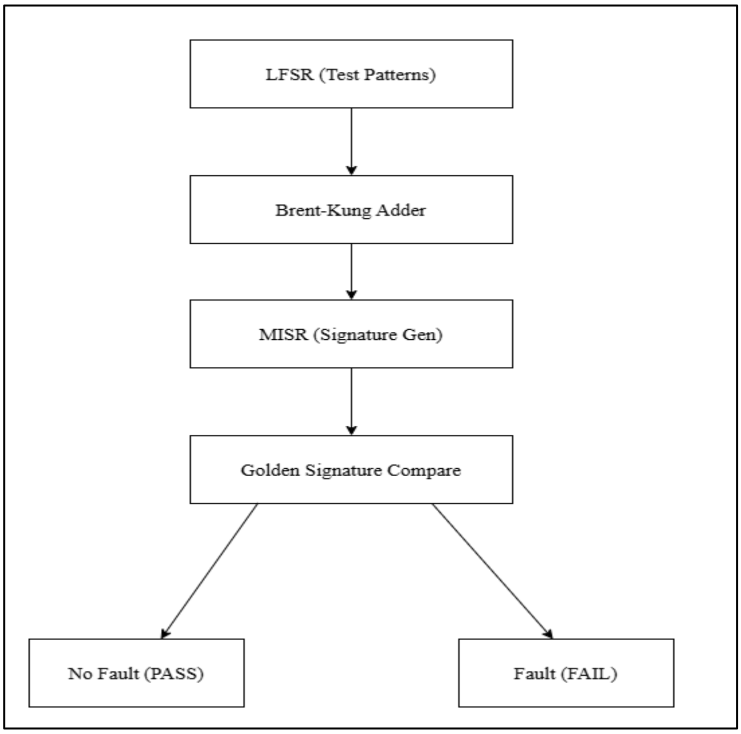

Figure 5. Overall Architecture

The LFSR generates pseudo-random test patterns, which are fed into the Brent-Kung Adder for processing. The adder's output is then compressed using a MISR, producing a signature that is compared with a precomputed Golden Signature. If the signatures match, the circuit is fault-free (PASS); otherwise, a fault is detected (FAIL). This self-testing mechanism automates fault detection, reducing hardware costs while ensuring efficient and high-speed testing.

5. Results and Discussions

The Verilog simulation waveform in (Figure.6) demonstrates the operation of a Fault-Resilient Brent-Kung Adder integrated with an BIST Architecture. The inputs A[3:0] and B[3:0] change dynamically, simulating different four-bit binary values fed into the adder across multiple clock cycles. For example, at 10 ns, A takes the value 5 (0101), and B takes A (1010). The carry-in (Cin) remains high (1), ensuring the adder consistently processes carry propagation during multi-bit additions, a critical factor in accuracy and performance.

At 20 ns, when A = C (1100), B = 3 (0011), and C_{in} = 1, the adder correctly produces a sum of F (1111) and a carry-out (C_{out}) of 1, confirming the correct arithmetic logic. The continuous variations in input yield consistent

sum and carry outputs, showcasing the Brent-Kung adder's efficiency in handling multi-bit additions and varying conditions. The BIST architecture is actively generating a signature[3:0] output, which shifts between distinct values such as 1, 2, 4, 8, and back to 1. This signature verifies that the BIST is performing internal self-checks to detect potential faults during operation. The periodic evaluation of internal states helps identify faults promptly, making the system robust against errors and highly reliable. The Brent-Kung Adder demonstrates both fault resilience and accurate arithmetic performance through its advanced BIST system. This design makes it suitable for critical applications, where reliability is paramount, such as aerospace and cryptography. The BIST ensures that faults are detected and mitigated, ensuring continuous operation even in error-prone environments.

The junction temperature is 30.6°C, with a thermal margin of 69.4°C, indicating sufficient thermal headroom. No off-chip power is supplied, and the effective θJA is 1.0°C/W. These power insights help in evaluating the efficiency and thermal feasibility of the design for FPGA implementation.

The utilization report (Table.II) shows that the design uses minimal FPGA resources, with only 5 LUTs (0.01%) and 8 Flip-Flops (0.01%) out of the available 230,400 and 460,800, respectively. The IO usage is 20 (5.56%) out of 360, indicating a relatively higher percentage compared to logic resources. Additionally, one BUFG (0.18%) is used from the available 544. The low utilization suggests that the design is lightweight and does not heavily tax the FPGA resources, leaving ample room for expansion or additional functionality.

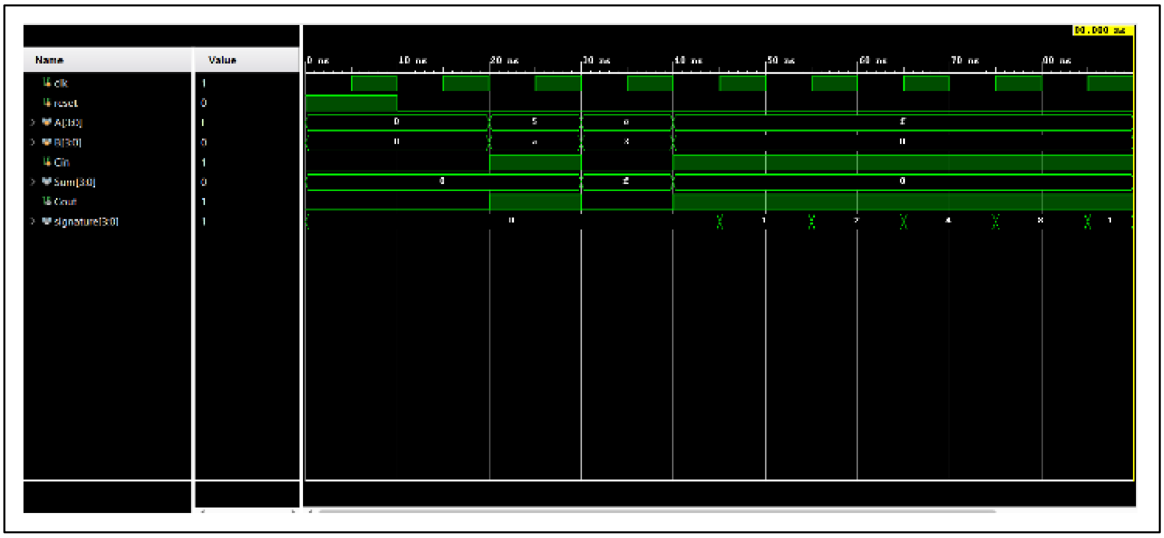

Figure 6. Simulation Result

The simulation waveform validates the Fault-Resilient Brent-Kung Adder by confirming its functional correctness, error detection capability. The correct operation of inputs (A[3:0], B[3:0], and Cin) and expected outputs (Sum[3:0] and Cout) ensures accurate addition. The signature [3:0] signal aids in fault detection, indicating error resilience. Proper clock and reset behaviour ensure stable operation, while propagation delays remain optimal for high-speed performance. The presence of expected transitions confirms that the adder maintains reliability.

Table 1. Power Analysis

Power	Values
On-Chip Power	5.761W
Dynamic Power	5.140W
Static Power	0.620 W

The total on-chip power consumption is 5.761 W, with dynamic power contributing 5.140 W (89%) and static power at 0.620 W (11%).

Table 2. Utilization Report

Resource	Utilization	Utilization %
LUT	5	0.01
FF	8	0.01
IO	20	5.56
BUFG	1	0.18

The schematic represents a Fault-Resilient Brent-Kung Adder Design (Figure.7) with Built-In Self-Test (BIST), integrating LFSR-based test pattern generation and MISR-based fault detection. The inputs (A[3:0], B[3:0], and Cin) pass through input buffers (IBUFs) before being processed by the Brent-Kung Adder, which consists of LUT-based logic for efficient addition. The sum and carry-out (Cout) results are then passed to a Multiple Input Signature Register (MISR), which compresses the outputs into a signature for fault detection.

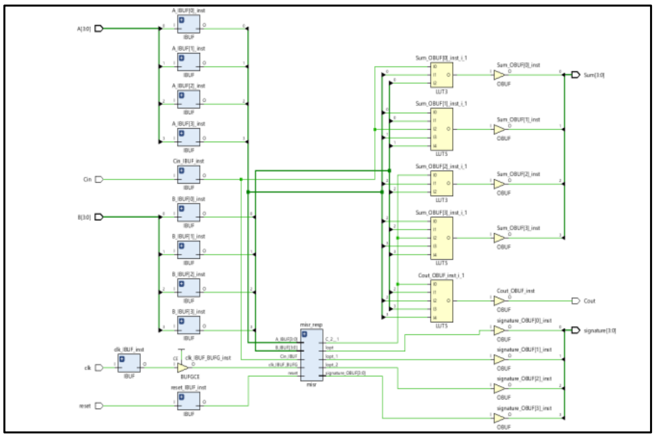

Figure 7. Schematic Diagram

The system operates synchronously using a buffered clock signal (clk), while a reset signal ensures proper initialization. The computed sum, carry-out, and signature are sent through output buffers (OBUFs) for further processing. By comparing the generated signature with a predefined golden signature, the system can determine whether the adder is functioning correctly or if faults are present, ensuring fault resilience through BIST methodologies.

6. Conclusion

The Fault-Resilient Brent-Kung Adder design using advanced Built-In Self-Test (BIST) Architecture successfully addresses the critical challenges associated with fault tolerance in digital circuits. The research effectively combines the efficient parallel processing capabilities of the Brent-Kung adder with the robustness of BIST, enabling the detection and diagnosis of faults in real time. The low resource utilization reported indicates that the design is not only efficient but also leaves room for future enhancements or integration with more complex systems. The managed power consumption and favorable thermal performance further validate the design's practicality for implementation in modern electronic devices. Overall, this research demonstrates a significant step forward in creating reliable arithmetic units that can withstand operational challenges, thereby contributing to the advancement of fault-tolerant computing in high-performance applications. The outcomes pave the way for further research and development, potentially leading to more sophisticated architectures capable of addressing the ever-growing demands of digital systems.

7. Future Work

There is potential to further enhance the fault resilience and efficiency of the Brent-Kung Adder by exploring advanced BIST techniques. This could involve integrating power-aware BIST mechanisms to reduce energy consumption during testing or adopting adaptive test pattern generation to increase fault detection precision while minimizing overhead. Additionally, incorporating machine learning algorithms for dynamic fault prediction and analysis could improve the adder's ability to identify complex, intermittent faults. Scaling the design to support higher bit-width adders with minimal impact on area and performance would also broaden its applicability in high-speed and large-scale digital systems.

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