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Optimized Double Tail Comparator based ADC for High Speed and Low Power Applications

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Abstract

Dynamic regenerative comparators are being used to increase speed and power efficiency in response to the need for ultra-low-power, area-efficient, and high-speed analog-to-digital converters. This study suggests using two transistors to create a low power double-tail comparator for the Flash Analog-to-Digital Converter. Designing a comparator and thermometer code to binary code converter at low supply voltage and low power dissipation is a challenging task in the creation of a low power Flash ADC. The primary goal is to construct comparators in order to achieve a high-speed Flash ADC. We should design each comparator to have a lower total power consumption because the comparators in Flash ADC are power-hungry components. Here, a low-power dynamic comparator is being designed. Next, we used a 2:1 MUX based on pass transistor logic to construct an encoder block. We have constructed a 5-bit Flash ADC using these components. To lower the Flash ADC's power consumption, a comparator and encoder are implemented utilizing dynamic CMOS circuitry. The Tanner EDA back-end tool is used to run the simulation.

Keywords: Tanner EDA, Comparator, Flash ADC, Encoder, Multiplexer, and Dynamic Double Tail.

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1. Introduction

In modern Very Large-Scale Integration (VLSI) technology, the demand for high-speed, low-power, and area-efficient Analog-to-Digital Converters (ADCs) has grown significantly, particularly in applications such as wireless communication, high-speed data acquisition, and radar systems. Among various ADC architectures, Flash ADCs are widely utilized for their high-speed parallel conversion; however, their traditional implementation suffers from excessive power consumption and large silicon area due to the extensive use of a resistive ladder network and a large array of comparators. To address these limitations, this work proposes an Optimized Double-Tail Comparator-Based Flash ADC, which integrates a modified double-tail dynamic comparator to enhance speed, reduce power dissipation, and improve overall efficiency. Unlike conventional Threshold Inverting Quantization (TIQ) comparators, the proposed design minimizes high-power-consuming components, leveraging dynamic CMOS logic to achieve optimized switching speed and power efficiency. This architecture ensures lower static power dissipation, making it highly suitable for high-performance VLSI applications where power and speed are critical design constraints. The suggested Flash ADC has been built and simulated with Tanner EDA tools, confirming its efficacy in low-power, high-speed digital signal processing applications. This work demonstrates a compact and power-optimized ADC architecture, making it an ideal solution for next-generation high-speed VLSI-based systems.

2. Literature Survey

The optimization and design of comparators in high-speed and low-power analog-to-digital converters (ADCs) have received tremendous research attention, especially in the context of mixed-signal system applications, IoT, and biomedical implants. The fundamental concepts of CMOS VLSI design principles are comprehensively covered by Weste and Harris [1], which serve as a reference for comparator and ADC circuit design. Kapaka et al. [2] concentrated on the design and verification of a low-power, high-speed flash ADC for mixed-signal designs, highlighting the significance of robust architecture for achieving a balance between speed and energy efficiency. Supporting this, Lund [3] provided an overview of comparator needs for high-speed ADCs, highlighting features like delay and metastability. Comparator design developments have heavily relied on double-tail dynamic architectures. Kumar et al. [4] introduced a double-tail comparator that provides enhanced performance for

high-speed ADC usage through power reduction and response time improvement. Likewise, Gao et al. [5] outlined several design methods for dynamic comparators, offering an extensive framework for energy reduction without compromising signal integrity.

Yang [6] further emphasized the role of design improvements in achieving the speed requirements of contemporary ADCs, especially for sampling high-frequency signals. Chitti et al. [7] applied a flash ADC based on a double-tail comparator, where significant improvements in speed and power efficiency were obtained, while Tyagi et al. [8] optimized the operation of a SAR ADC based on a dynamically controlled comparator in 45nm technology, oriented towards biomedical and IoT applications. Thai et al. [9] demonstrated an 8-bit flash ADC with a double-tail comparator implemented on a 180nm CMOS process with a small area and low power consumption, suitable for embedded sensors. Vaithiyanathan et al. [10] compared dynamic comparator circuits, considering the best trade-offs between high speed and low power, specifically focusing on layout-driven optimizations.

A thorough survey of comparator architectures was conducted by Mehra et al. [11], elaborating on the design issues and performance tendencies in various technologies and applications. Finally, Sahana and Dwivedi [12] proposed a double-tail dynamic comparator optimized for 90nm technology with the aim of reducing power consumption and enhancing switching speed for integration into high-speed ADCs.

3. Architecture of Flash ADC

An N-bit flash ADC requires 2N-1 comparators to be implemented. Each comparator, like an operational amplifier, has two inputs: the inverting input receives the analog signal, while the non-inverting input receives a reference voltage. These comparators are arranged in connection with a resistive ladder network, which divides the reference voltage. This ladder is made up of 2N resistors for an N-bit ADC, whereas 32 resistors are needed for a 5-bit flash ADC.

In order to provide evenly spaced reference levels that differ by one least significant bit (LSB), the resistive ladder is linked between a reference voltage and ground. The analog input signal is compared to its respective reference voltage by each comparator, which outputs a high logic level if the analog input exceeds the reference level and a low logic level otherwise. The

combined outputs of the comparators provide a thermometer code, which is subsequently translated into binary.

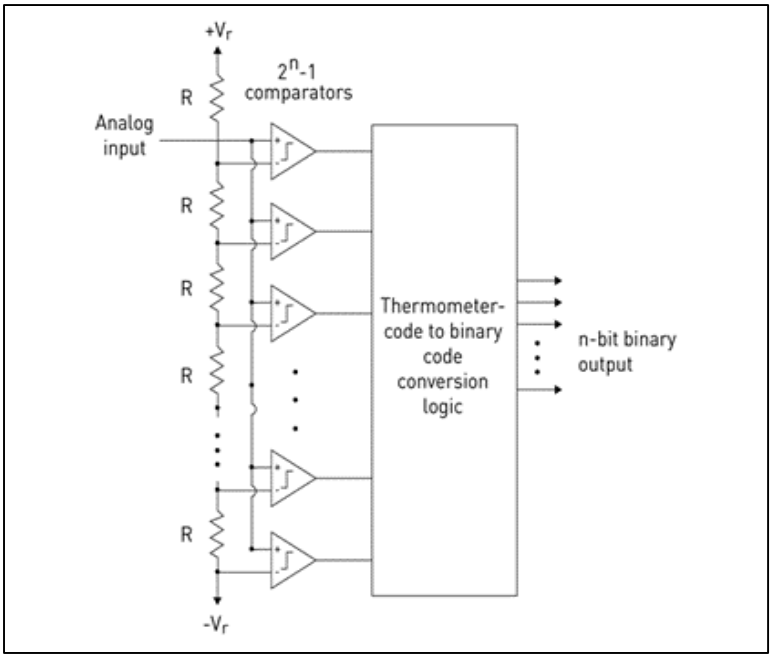

Figure 1. Flash ADC

A resistive ladder network is utilized in a 5-bit flash ADC to supply the comparators with steady reference voltages. The architecture of an N-bit flash ADC requires the use of 2N resistors, which make up this network. The primary role of the resistive ladder is to distribute the reference voltage evenly across the resistors, creating incremental reference levels. This arrangement ensures that the difference in reference voltage between any two adjacent comparators equals the value of the least significant bit (LSB), enabling precise comparison with the input signal.

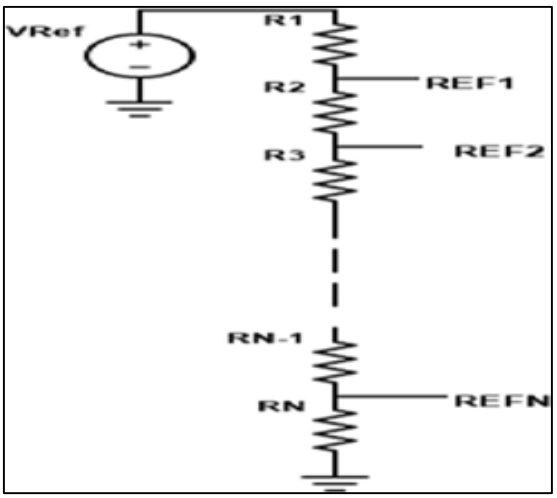

Figure 2. Resistive Ladder Network

3.1 Comparator

Comparators are the key building blocks of a Flash Analog-to-Digital Converter (Flash ADC), which converts analog input signals into digital codes. A Flash ADC produces a set of reference voltages through a voltage divider network, usually built with resistors. The analog input signal (Vin) is compared against a specific reference voltage (Vref) by each comparator.

A logic 1 is generated by the comparator when Vin>Vref, and a logic 0 when Vin<Vref.

The ADC employs 2N−1 comparators, where each comparator corresponds to a particular reference voltage.

4. Existing System

Three CMOS inverter topologies are integrated into a self-tuning structure in the topology presented herein. Here, the threshold voltage of the inverter is dynamically tuned using a DC feedback loop. The following is a description of how the self-tuning mechanism works:

A resistive divider consisting of resistors R0R_0 and R1R_1 sets the threshold voltage for the master and slave inverters. The core component of a threshold-compensated TIQ-comparator is the master inverter, which is joined to the power rails via an NMOS and a PMOS transistor. These transistors generate a negative feedback mechanism when they are operating in linear (or triode) regions. The master inverter output controls their gate terminals, thus modulating their resistance according to the inverter output voltage. This method allows the transistors to behave as voltage-controlled resistors.

Both the master and slave inverters have the same aspect ratios. With the input of the master inverter at the desired switching threshold voltage, it produces a control voltage. This controls the resistance of the NMOS and PMOS transistors on the power rails to allow them to self-compensate. The negative feedback loop of the circuit ensures that, despite process or temperature variations, the switching thresholds of the master and slave inverters remain constant.

In order to reduce power consumption, another PMOS transistor is added to the design. This transistor, actuated by a clock signal (CLK), breaks the path of power supply between

VDDV_{DD} and ground, if required, essentially lowering the power consumption of the circuit. The process is schematically depicted in the schematic diagram.

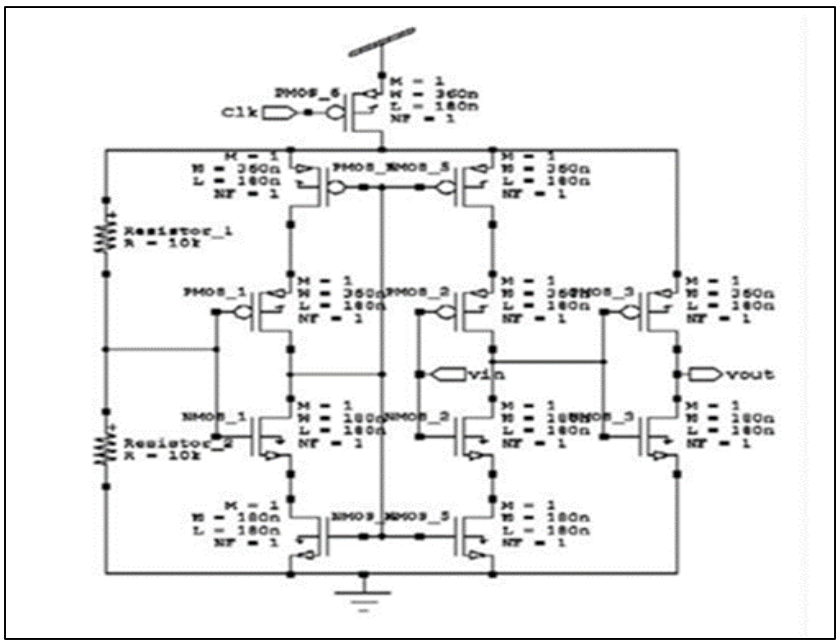

Figure 3. TIQ Comparator

5. Proposed System

5.1 Traditional Double-tail Comparator

The speed, precision, and power efficiency of the double-tail comparator are all well balanced.

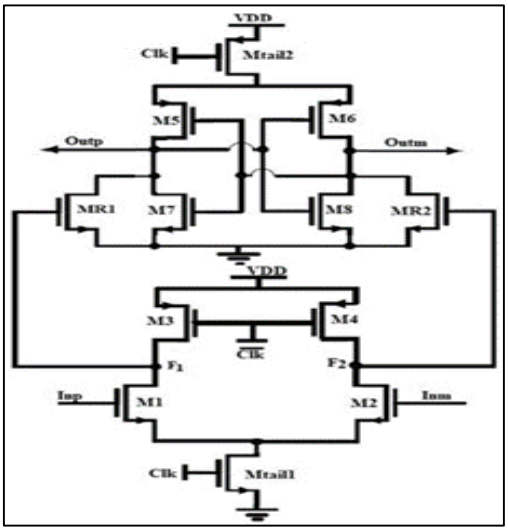

Figure 4. Conventional DoubleTail Dynamic Comparator

By reducing offset voltage through careful design and achieving fast transitions with minimal delay, it ensures reliable performance in high-speed ADCs and other time-critical systems. Its ability to conserve energy while maintaining high precision makes it a preferred choice for both performance-critical and energy-sensitive applications. This versatility underscores its importance in modern electronics, particularly in devices where power and speed are equally critical.

Drawbacks in the previous system:

- The higher transistor count in the double-tail design can add complexity to the circuit design, making it potentially more challenging to optimize and integrate.
- More transistors typically mean higher power consumption due to increased leakage currents and more complex circuitry, leading to greater power dissipation.
- The added transistors and complexity can introduce additional delay, which might reduce the overall switching speed compared to a more streamlined design.

5.2 Optimized Double Tail Comparator

To solve the problems of speed, area efficiency, and power consumption, the Double-Tail (DT) comparator was created, which was a ground-breaking advancement in the field of analog-to-digital converters (ADCs). A more simplified DT comparator design with fewer transistors 12 instead of 16 was introduced by rethinking the architectural structure of a conventional comparator. Through optimization, the comparator's silicon area is reduced, and parasitic effects that could impair its performance are minimized. As such, it offers an effective circuit suitable for use in contemporary small, low-power electronic systems.

The best DT comparator innovation is its two-edge triggering, where both falling and rising edges of the clock signal drive the outputs. This doubles the speed at which the comparator can operate compared to single-edge comparators. Handling both edges of the clock is particularly beneficial in high-speed ADCs, where both speed and accuracy must be high. The DT comparator is thus tailored to satisfy the stringent specifications of high-speed applications without the need for a power boost. A switching mechanism is controlled by a

specially designed system for driving the DT comparator. M1 and M7 transistors are deactivated while M6 and M8 transistors are activated when the clock signal is asserted. The transistors, however, assume reverse duties when the clock is deasserted. This process of switching generates a differential voltage based on the input signals, which is utilized to determine the output. Timely control of the switching process renders the comparator high speed and accurate with low power dissipation.

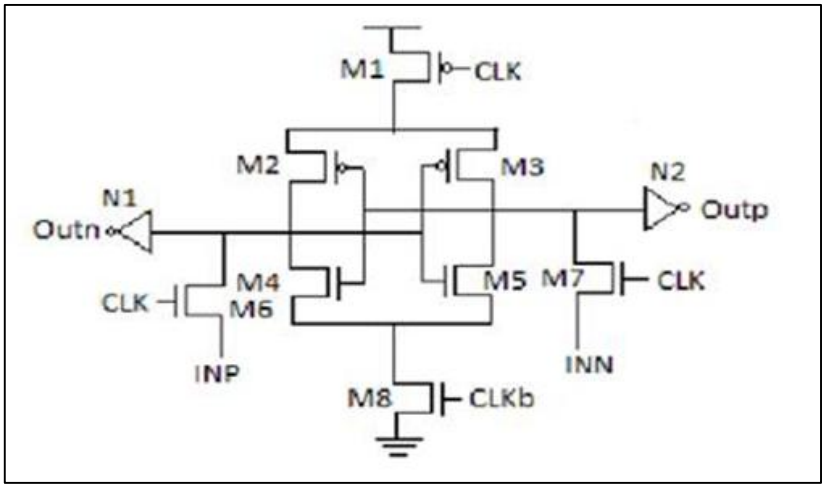

Figure 5. Optimized Double Tail Comparator

Power efficiency is the signature characteristic of the DT comparator. Its low transistor count, along with dynamic CMOS logic use, guarantees minimal power consumption even at low supply voltages. The DT comparator is thus most appropriate for battery-operated systems and applications where energy efficiency is crucial. Operating efficiency at low supply voltages further extends its application to nearly any power-restricted environment, ranging from handheld devices to embedded systems. The compact nature of the DT comparator is a major contributor to the performance of the ADC, as well as its power and speed benefits. The comparator conserves silicon area, minimizes architecture, and simplifies design by reducing the number of transistors used in operation. The compactness offers greater functionality in less space and is best suited for applications where physical space is limited.

The DT comparator represents a breakthrough in ADC design that balances power, speed, and area efficiency precariously. The new features, such as double-edge triggering and optimal transistor structure, set a new benchmark for comparator performance. By overcoming some of the most significant design challenges, DT comparator opens the door to future high-speed, low-power ADCs to meet the growing needs of complex electronic systems.

5.3 Used Method Advantages

Simplified Design: It leads to fewer transistors and hence a simpler and less complex design. This results in lower complexity in the layout and easier integration into a larger circuit.

Less Power Consumption: Power usage is lower with fewer transistors. The design can be optimized to consume less power, which is advantageous in power-sensitive applications.

Lower Area Requirement: The reduced number of transistors means less silicon area. This corresponds to a smaller design size, which is a significant advantage in the case of integrated circuits with limited area.

Smoother Operation: With the removal of parasitic capacitances, the new transistor structure will enable the 12-transistor design to achieve smoother operation. This is because there will be less interference from external factors such as capacitance in the circuitry.

5.4 Multiplexer (Mux) Based Encoder

The output of thermometer code, a novel binary encoding technique, resembles a thermometer reading, thus the name. As the encoded value rises, the number of '1's in the code increases, similar to how mercury rises in a thermometer as the temperature goes up. Various encoders can convert thermometer code to binary, such as Wallace tree encoders, encoders using multiplexers (MUX), XOR-based encoders, and ROM-based encoders, each offering distinct pros and cons. In this project we have used a MUX-based encoder. The block diagram of a 2x1 MUX is shown in the figure 6.

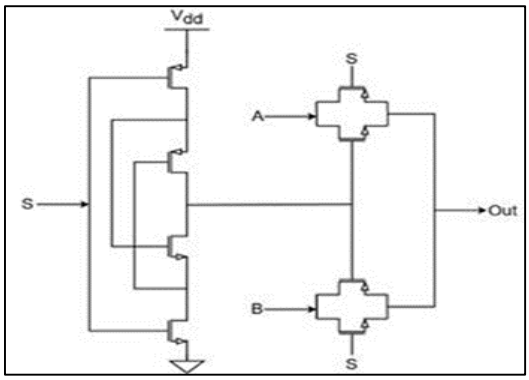

Figure 6. 2X1 MUX Block Diagram

It is a 2:1 MUX-based encoder that has 31 inputs and 5 outputs. The thermometer code is converted to binary code. This encoder has twenty-six 2X1 MUXs.

6. Results and Discussion

The TANNER tool is used to design and simulate circuits in 250 nm technology. Compared to the current Flash ADC, speed and power consumption are reduced.

6.1 Encoder based on MUX

As seen in Fig. 7, the encoder is developed using transmission gate logic and uses the MUX to minimize power consumption.

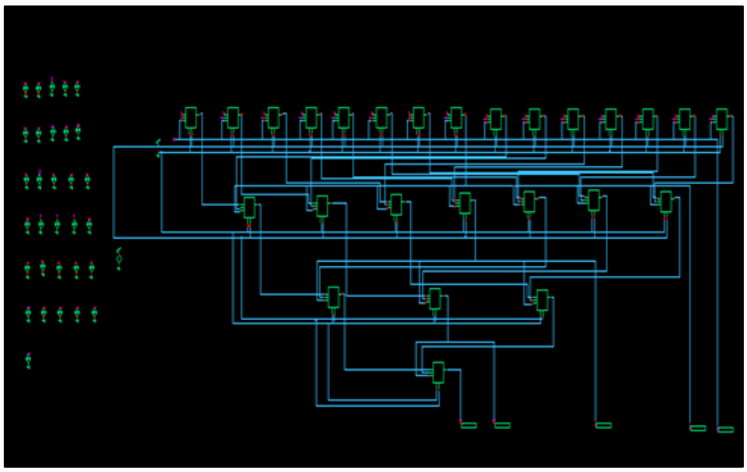

Figure 7. Diagram of a MUX-Based Encoder

6.2 The Flash ADC

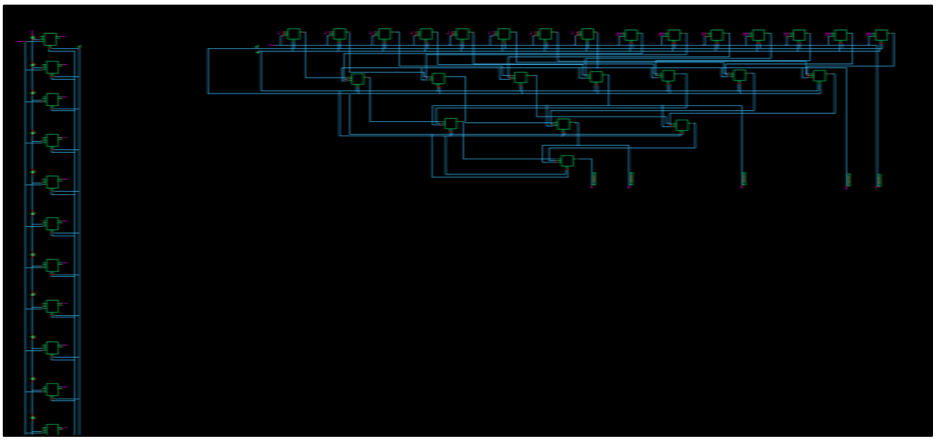

Figure 8. Diagram of Flash ADC

As seen in Fig. 8, the flash ADC architecture makes use of a MUX-based encoder and a dynamic doubletail comparator. Additionally, Fig. 9 displays the circuit's findings.

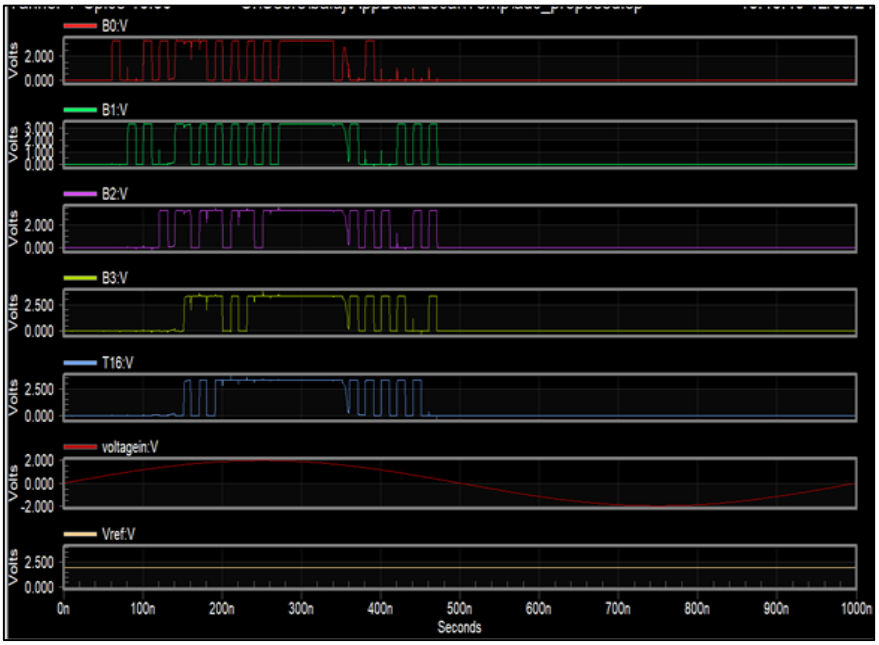

Figure 9. Output of 5-bit ADC using Modified Double-Tail Comparator

Table 1. Comparative Analysis of Proposed Work with Existing Literature

Parameters	Flash ADC Using TIQ	Flash ADC using Modified Double-Tail Comparator Technology
Technology	250nm	250nm
ADC Resolution	5-bit	5-bit
Voltage Supply	3V	3V
Area	614	801
Power	12.704mW	9.27mW
Convention Time	12.84Sec	7.59Sec

7. Conclusion

The shortcomings of the TIQ comparator, including its high-power consumption and process fluctuations, are addressed by the suggested Flash ADC architecture, which incorporates a modified dynamic comparator. It provides quicker operation, reduced power

dissipation, and a compact architecture by counting fewer transistors and using double-edge triggering. Using dynamic CMOS logic improves noise immunity, reduces static power, and increases efficiency. Because of these improvements, the ADC is perfect for energy-sensitive applications such as medical systems, portable electronics, and Internet of Things devices.

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