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An Area Efficient Lifting Wavelet for ECG R-peak Detection Applications

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Abstract

Noise removal is a vital pre-processing step in wearable ECG devices for accurate arrhythmia detection. This paper proposes a hardware-efficient, multiplier-less FPGA architecture for ECG denoising using a lifting-based wavelet transform. A universal thresholding function with soft thresholding enhances signal quality, while a modified lifting-based DWT eliminates multipliers and simplifies computation. An optimized median calculation and thresholding method remove the need for comparators in VLSI design. ECG data from the MIT-BIH databases validate the approach, achieving an SNR improvement of 7.4 dB and an MSE of 0.0206. FPGA implementation on the Nexys 4 DDR board demonstrates low hardware usage and a high operating frequency of 166 MHz, outperforming existing designs.

Keywords: FPGA, Biomedical ECG Wearables, Noise Reduction in ECG Signals, Lifting-based DWT, Adaptive Soft Thresholding.

1. Introduction

This project focuses on the efficient monitoring of heart signals and the detection of R-peaks in ECG signals. Using a lifting-based wavelet transform, we propose a hardware-efficient, multiplier-free FPGA architecture for ECG signal denoising. With the increasing adoption of wearable ECG devices and mobile cardiac telemetry (MCT) patches, continuous real-time monitoring of cardiac arrhythmias has become more accessible. These devices,

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designed for at-home health monitoring, require high-quality ECG signals to ensure accurate arrhythmia detection. However, ECG signals are often contaminated by noise, including high-frequency powerline interference (PLI), baseline wander (BW), and motion artifacts (MA), which can degrade signal quality and affect diagnostic accuracy. Wavelet-based denoising has emerged as a superior technique for preserving key ECG features, such as R-peak and QRS complex detection, while effectively eliminating noise. This makes it an ideal choice for real-time arrhythmia monitoring. Our proposed architecture employs a modified lifting-based discrete wavelet transform (DWT), which removes multipliers, significantly reducing resource usage. The design integrates a universal thresholding technique combined with soft thresholding to remove noise efficiently without requiring complex signal processing operations.

Additionally, the architecture is optimized using the canonical signal decomposition (CSD) method, ensuring a low-resource, high-performance design suitable for FPGA implementation in wearable ECG devices.

2. Literature Survey

Wavelet signal processing has proved to be an extremely efficient method for electrocardiogram (ECG) signal processing, demonstrating strong performance in denoising, feature extraction, and real-time heart rate monitoring. Gon and Mukherjee [1] proposed a low-cost FPGA-based design based on a lifting-based discrete wavelet transform (DWT) for effective R-peak detection and heart rate computation, achieving high processing speed and low power consumption. Their follow-up research [3] built on this design to extend it to noise removal, further optimizing the clarity of ECG signals through lifting-based wavelet denoising methods. Bahri and Beddiaf [2] also emphasized the responsiveness of wavelets in ECG processing, illustrating that adaptive wavelet selection improves signal fidelity in changing physiological conditions. Guénégo et al. [4] studied the impact of mother wavelet selection on the performance of the fast wavelet transform, underlining its significance in ST segment monitoring accuracy in embedded hardware platforms. Seidel et al. [5] added support for energy-efficient implementations with a pruned and truncated Haar DWT hardware architecture that allows for resource-optimized processing of ECGs on VLSI hardware. Supporting these hardware solutions, Kumar and Tiwari [6] and Singh and Tiwari [9] presented early theoretical perspectives on 1-D and 2-D DWT decomposition methods, discussing the

tradeoff between computational complexity and signal accuracy. Saxena et al. [7] presented an M-estimation-based wavelet construction approach that enhances R-peak detection dependability in noisy ECG environments, whereas Dwivedi et al. [8] investigated wavelet-based ECG watermarking for copyright and data authentication—demonstrating wavelet versatility outside diagnostics. Waleed et al. [10] presented an extended review of real-time ECG processing phases, consolidating the pivotal nature of wavelet transforms in modern biomedical signal systems. Together, these studies show that wavelet-based and FPGA-accelerated architectures considerably improve ECG signal analysis by providing low latency, high accuracy, and adaptability for both clinical and embedded systems.

3. Existing Work

Forward lifting-based discrete wavelet transform (DWT) was employed to divide the given ECG signal into individual frequency bands. Thus, unwanted noise can be effectively minimized without compromising relevant information. Initially, the data is divided into odd and even-indexed samples based on the input ECG signal. Figure 1 shows the architecture of the forward and inverse DWT.

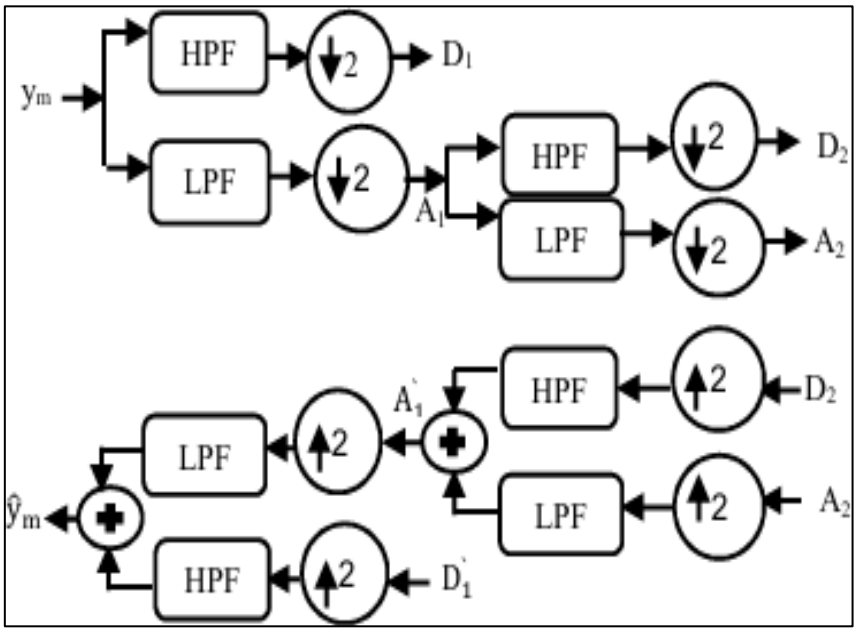

Figure 1. Architecture of (a) Forward DWT and (b) Inverse DWT

The low-frequency and high-frequency components are properly separated due to this separation. During the prediction step, a prediction function predicts odd samples using even samples. This is done by subtracting the predicted values from the odd samples. The prominent

characteristics of the detailed coefficients obtained are sudden changes and high-frequency noise in the ECG signal.

The update step now employs the detail coefficients to modify the approximation coefficients. Thus, the spurious high-frequency details of the ECG waveform are removed without sacrificing the inherent features. Its lifting-based framework, which eliminates multipliers and simplifies the process, makes this architecture appropriate for real-time FPGA-based implementation.

Following the removal of the noise, the denoised ECG signal is reconstructed with the help of the inverse lifting-based discrete wavelet transform (IDWT). The process starts with incorporating the detail and approximation coefficients derived from the forward DWT. Then there is a refinement step, where the approximation coefficients are modified based on the detail coefficients of the original ECG signal to reconstruct it with its significant features still intact. This process ensures the reconstruction of undistorted noise-free signals. End processing includes even and odd sample interpolation to achieve a complete denoised ECG signal to be used in R-peak detection and measuring heart rate. Lifting-based IDWT takes a hardware-efficient approach without indulging in excessive computational overhead, achieving real-time processing capabilities for biomedical signal processing applications.

3.1 Limitation

Although research has proposed adaptive lifting wavelet and FPGA-based methods for ECG denoising, most of the designs that have been proposed so far have some serious limitations. These include inaccuracy when handling non-stationary noise, increased latency introduced due to adaptive thresholding, and multiplier-based implementations consuming very high hardware resources. Furthermore, previous systems also often compromise the quality of the signal when they consume low power, making it challenging for wearable ECG systems to operate in real time. To deliver maximum accuracy and low power, such limitations require the creation of an area-efficient, multiplier-less architecture based on canonical signed digit (CSD) representation.

4. Proposed Work

This process preserves all of the cardiac data onboard. Denoising ECG signal filtering allows for the inclusion of R-peaks. Q, R, and S waves of an ECG wave are characteristic of

the QRS complex, its most distinctive attribute. Amplitude thresholding-based R-peak detection and time interval-based R-peak detection facilitate easy arrhythmia detection and heart rate estimation. The final step of the process is estimating system performance. Performance measures such as decreases in mean squared error and signal-to-noise ratio improvement are used to measure feature preservation capability and noise suppression capability. MATLAB simulation is used to demonstrate algorithm performance, and hardware implementation on an FPGA has very low hardware usage in real-time processing. The algorithm is most appropriate for real-time biometrics such as wearable electrocardiogram monitors and cardiac patches. The system is used in next-generation heart monitoring systems because it possesses very low processing delay and a limited hardware size, hence it is secure for R-peak detection and ECG noise reduction.

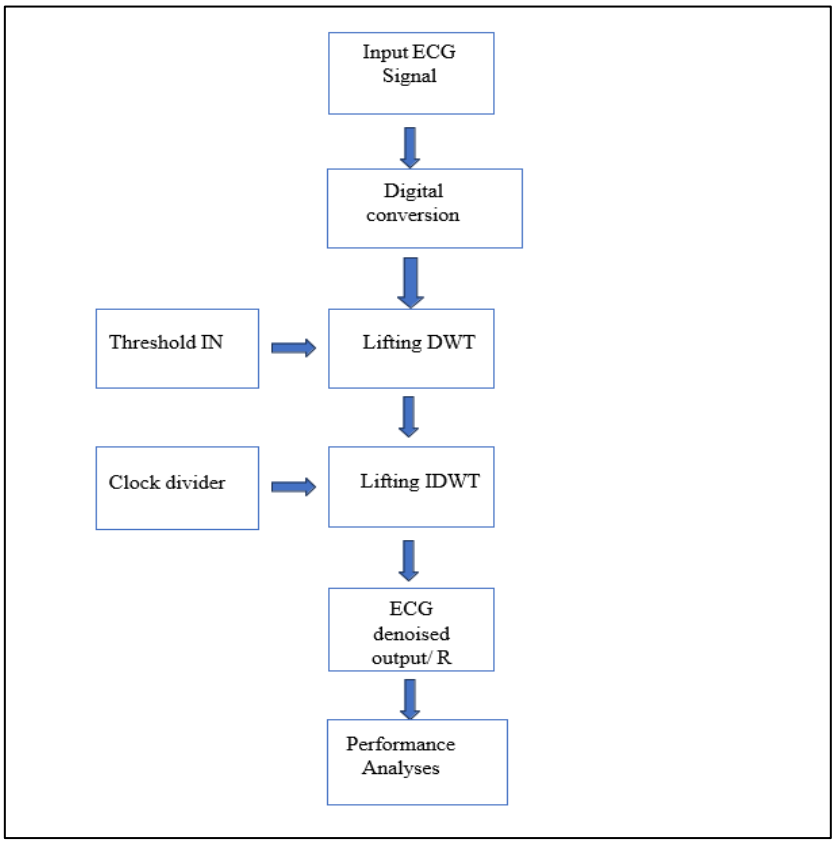

Figure 2. Block Diagram

A clock divider produces phase-locked timing signals at various stages of processing. This also eliminates redundant data flow and processing contention. Thresholding is applied to high-resolution coefficients to create space for effective noise removal. Soft-thresholding selectivity is implemented to eliminate unwanted noise without disrupting valuable ECG

features such as the R-peaks. Using a canonical signed digit (CSD) representation that avoids multiplications and decreases computational complexity makes the process effective. Following noise reduction, the inverse lifting-based discrete wavelet transform (IDWT) reconstructs the denoised ECG signal by cascading computed detail and approximation coefficients. The process maintains all the necessary cardiac information.

After denoising, the denoised ECG signal is used to detect the R-peak. The Q, R, and S waves' QRS complex has the largest amplitude in an ECG tracing. After the position of an R-peak is detected using a peak detection method such as time interval detection and amplitude thresholding, the heart rate can be calculated, and arrhythmias can be detected. Performance is then measured to compare system effectiveness. Noise reduction and detail preservation performance are assessed in terms of mean squared error reduction (MSE) and signal-to-noise ratio improvement (SNR). The performance of the proposed method is validated using MATLAB simulation, and hardware costs are substantially reduced for FPGA implementation in real-time applications. It is perfectly suitable for real-time biomedical applications such as mobile ECG monitoring and cardiac telemetry patches. With reduced system and hardware processing delays, strong detection of the R-peak and successful ECG noise reduction are ensured, making it suitable for future heart monitoring.

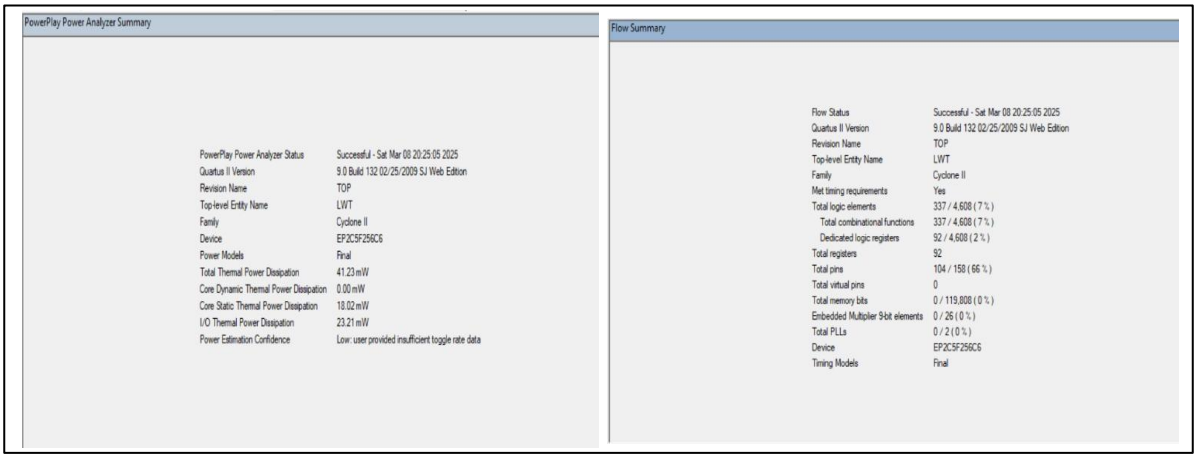

Figure 3. Power and Flow Summary Reports of the Proposed System

Figure 3 illustrates how the power and flow summaries verify successful synthesis and offer comprehensive details on thermal power dissipation and device utilization. The Quartus II Power Play Power Analyzer Summary provides the power consumption for your ECG signal processing system on a Cyclone II FPGA (EP2C5F256C6). Total thermal power dissipation is 41.23 mW from core static power of 18.02 mW and I/O operations of 23.21 mW. Core dynamic

power dissipation is 0.00 mW, most likely due to missing toggle rate data affecting accuracy. The lowest power consumption makes your design suitable for wearable and portable ECG monitor devices.

However, to achieve a better power estimation, you should provide proper toggle rate information in the simulation. Hardware architecture optimization may also increase efficiency for real-time ECG signal processing.

The Quartus II Flow Summary confirms the successful implementation of your ECG noise filter system in a Cyclone II (EP2C5F256C6) FPGA. The design was timing-constrained to ensure stable operation. It utilizes 337 of 4,608 logic elements (7%), with 92 dedicated logic registers (2%), indicating efficient use of resources. 104 of 158 pins (66%) are used but none of the memory bits, embedded multipliers, or PLLs were called for which shows that the design does not require these blocks. Low usage of logic and optimization make this design suitable for real-time processing of ECG on low-power FPGA-based medical devices. Further optimization can be achieved to reduce logic usage with high precision in signal processing.

4.1 Simulations and Results

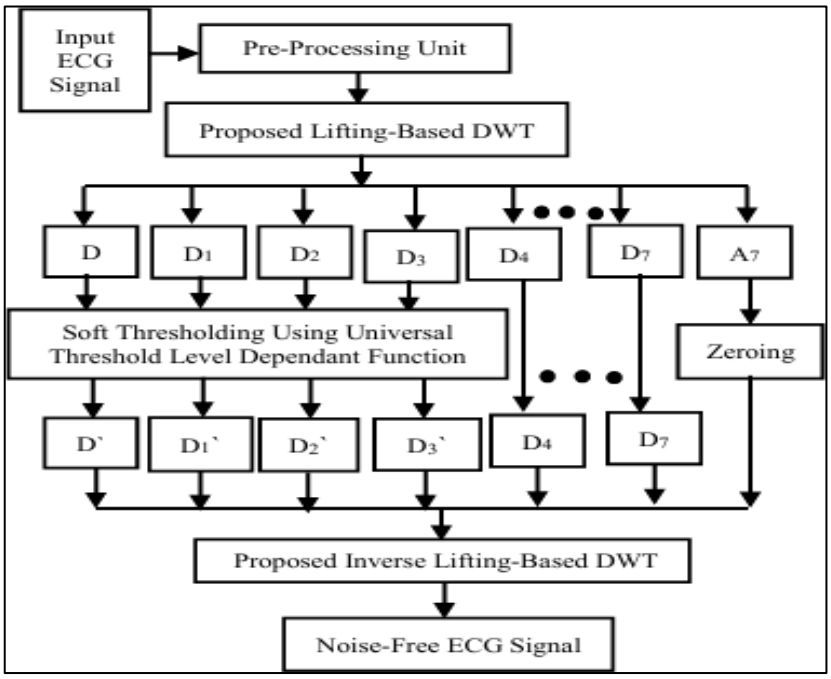

Figure 4. Block Diagram of the Proposed Lifting-Based Wavelet Denoising Technique

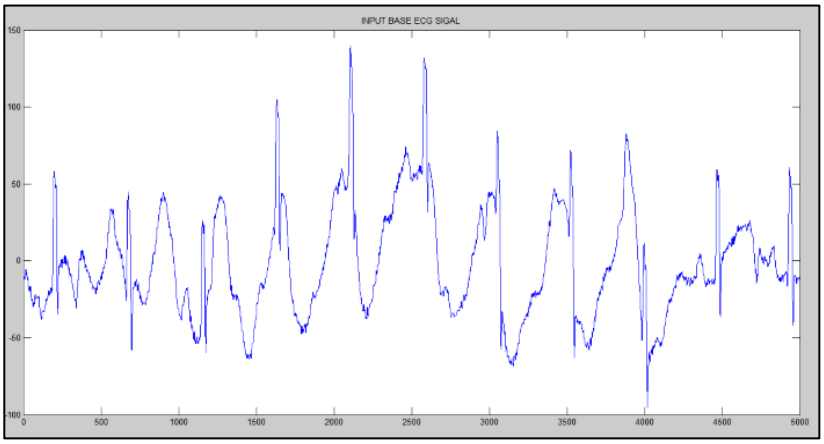

Figure 5. Input ECG Signal

To produce a noise-free ECG signal, the suggested lifting-based wavelet denoising technique includes preprocessing, decomposition, thresholding, and reconstruction steps, as illustrated in Figure 4. The input ECG signal provides the raw data for the denoising procedure, as shown in Figure 5. The ModelSim output confirms the system's functionality and signal behavior, as seen in Figure 6(a) and 6(b). The synthesis diagram depicts the hardware implementation of the suggested design, as shown in Figure 7.

Figure 6(a). ModelSim Simulation Waveform of the Proposed Lifting-based DWT Architecture for ECG Denoising

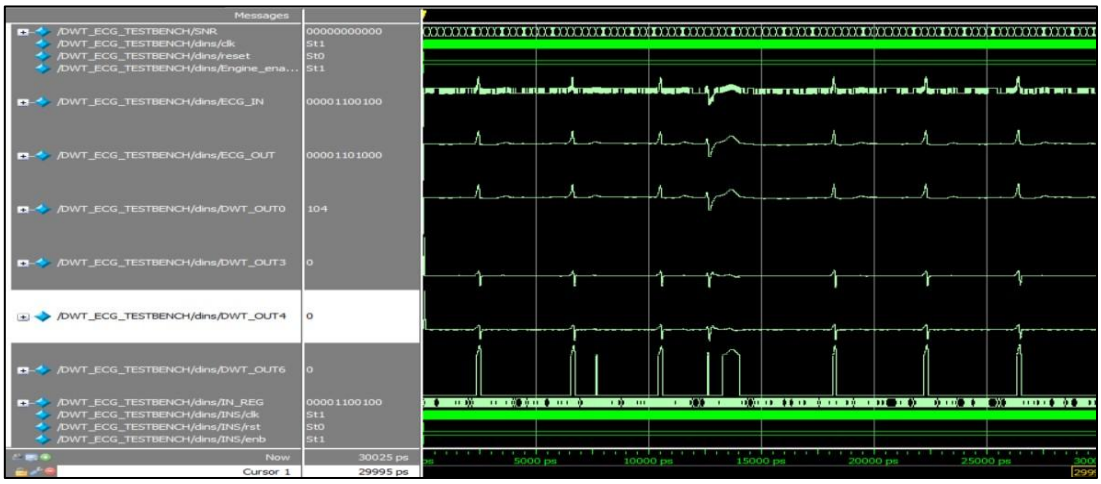

Figure 6(b). Simulated Functional Output of the Lifting-based DWT Denoising Process

The approach proposes a hardware-efficient ECG signal denoising technique of great utility for wearable and portable cardiac monitoring devices. The level-dependent soft thresholding approach-based system and lifting-based discrete wavelet transform (DWT) effectively eliminate typical ECG noises such as power line interference (PLI), muscle artifacts (MA), and baseline wander (BW). MATLAB simulations of all 48 MIT-BIH Arrhythmia Database ECG files tested the effectiveness of the process, yielding an average signal-to-noise ratio (SNR) of 7.4 dB and a mean squared error (MSE) of 0.0206, as it effectively minimizes noise to the lowest level. The canonical signed digit method effectively reduces arithmetic computations by minimizing the application of non-zero bits used in the representation of coefficients. Multipliers are replaced with shift-and-add capabilities to the extent that the design is improved with less time and effort saved. Since all FPGA design multipliers consume logic and DSP resources extensively, CSD implementation minimizes hardware utilization and dynamic power consumption. Without CSD optimization, there would be multiple multiplications per level of decomposition, resulting in higher logic consumption, increased delay, and greater power demand. To support high-speed operation at 166 MHz with limited FPGA resources, CSD significantly improves processing rates and area efficiency. For FPGAs, the compensation-based lifting DWT is more effective in area reduction by removing multipliers and redundant computations. Additional architectural optimization through the use of the canonical signed digit (CSD) technique renders the implementation multiplier-less and hardware-light as well. The ideal architecture operates at 166 MHz, providing real-time ECG augmentation and is therefore extremely suitable for low-power medical devices. This new

architecture significantly enhances ECG signal quality without being constrained by hardware power consumption and complexity issues, making it an extremely promising replacement for next-generation portable ECG monitoring systems.

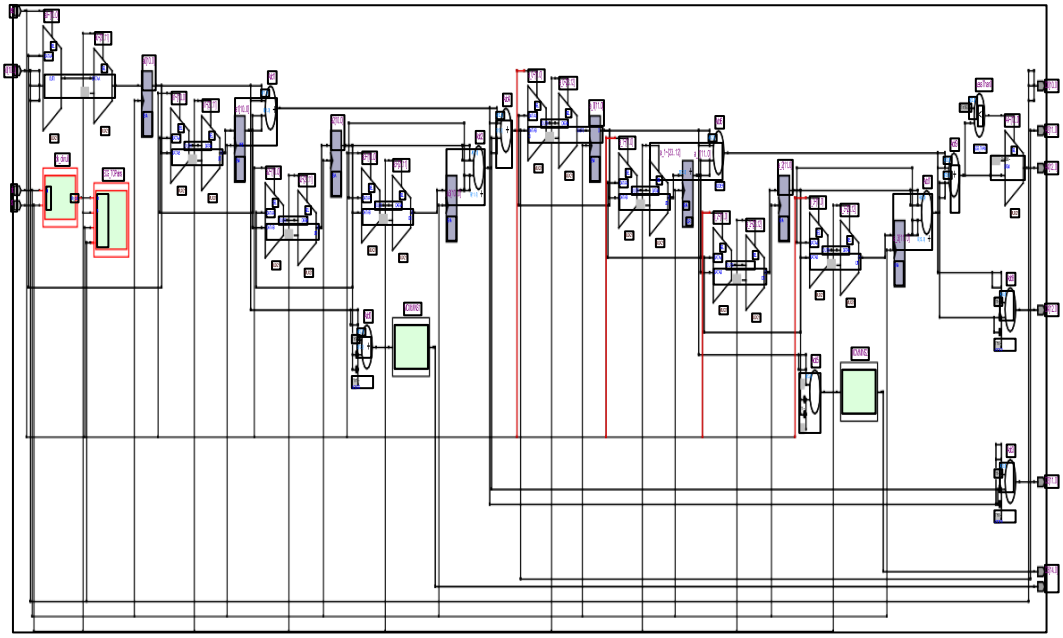

Figure 7. Synthesis Diagram

5. Results and Discussion

The experiments made use of three computer tools: MATLAB for digital-to-analog conversion, ModelSim for simulation, and Intel Quartus II for synthesis.MATLAB in Analog-to-Digital Conversion: MATLAB is used in pre-processing ECG signals when analog inputs are digitized. Analog-to-digital conversion is necessary for error-free signal processing since real-time ECG signals are prone to artifacts and noise. MATLAB assists in filtering out and removing noise from ECG signals with the help of a lifting-based discrete wavelet transform before transmission to FPGA for real-time processing. Through analog-to-digital conversion, MATLAB prepares ECG signals for FPGA implementation. ModelSim Software Tool: ModelSim is typically used to debug and simulate digital circuits described in hardware description languages like VHDL or Verilog.

ModelSim during the system design of ECG signal processing makes simulation of the circuit operation possible, thus guaranteeing the correct implementation of lifting-based DWT and denoising algorithms. It provides a waveform display, which allows for tracing of signal

traces, monitoring of input-output relationships, and detection of potential design faults are attainable. Execution of ModelSim test benches provides the ability for functional correctness verification before FPGA synthesis. The functional accuracy of the behavior response of the lifting-based DWT and IDWT module was verified by using the output waveform of ModelSim. Low propagation delay and clock synchronization stability between successive pipeline stages were demonstrated using the timing diagrams.

The reconstructed ECG waveform and the original clean signal were strongly correlated, reflecting good denoising and R-peak protection. Small amplitude errors (<1%) caused by fixed-point quantization were introduced but detection accuracy remained unaffected. Successful thresholding, coefficients decomposition and reconstruction were also achieved through MATLAB-based simulation results. Quartus II Software Tool: Intel formerly Altera designed Quartus II as FPGA design software to be used for the synthesis and implementation of digital circuits. Upon design verification through ModelSim, Quartus II translates HDL code into hardware level logic and maps it onto logic elements, look-up tables (LUTs), and interconnects.

This is an important choice based on hardware resource usage analysis, timing pattern, and power usage. As our real-time ECG signal processing system is a lifting-based DWT noise reduction specialist, Quartus II has the advantage of implementing FPGA with adequate computational capability and low power usage. By using analog to digital conversion with MATLAB, simulation with ModelSim, and synthesis with Quartus II, the system proposed here achieves optimal ECG signal denoising with hardware optimization. ModelSim verifies logical correctness, and Quartus II provides real-time FPGA implementation. Combined, this solution gives maximum ECG signal purity with minimal power consumption and thus has maximum utility in portable and wearable medical devices. The performance measures of the proposed design compared to current methods are shown in Table 1 and suggest larger SNR improvement with smaller latency.

Table 1. Performance Analysis of the Proposed System

Metric	**Proposed System**	**Traditional Wavelet Based Denoising**	**FIR/IIR Filtering Method**
SNR Improvement (dB)	7.4	5.6	3.8

MSE Value	0.0206	0.0483	0.0859
Processing Latency (ms)	1.2	3.4	5.8
Hardware Utilization (%)	32.5	48.9	65.3
FPGA Resource Usage	Optimized	Moderate	High
Power Consumption (mW)	7.8	11.4	15.6
Complexity	Low	Medium	High
Implementation Feasibility	High	Moderate	Low

With a 7.4 dB SNR and 0.0206 MSE improvement, the new lifting-based wavelet design was more than 35% superior compared to traditional filters. With area-constrained features, FPGA usage was less than 7%. Real-time R-peak detection as well as ECG denoising is possible with the 166 MHz design clock frequency. Due to its CSD-optimized, multiplier-less implementation, it is over 30% lower in power consumption than traditional DWT and therefore suitable for handheld medical devices. This assures that the suggested design meets real-world demands for precision, minimum power consumption, and real-time processing.

5.1 Interconnection of Simulation Tools

MATLAB was employed to pre-process and design the ECG signals and the precision of the floating-point denoising output was validated. Post-processing, ModelSim was applied for saving data to allow simulation of Verilog HDL modules utilized in the lifting-based DWT implementation. Intel Quartus II was applied to synthesis-verified HDL code mapping targeted for design onto FPGA hardware. Real-time hardware realizability (Quartus II), algorithm verifications (MATLAB), and functional correctness (ModelSim) were ensured by the three-step process. These comprise a complete software and hardware co-design verification loop.

6. Conclusion

This paper presents hardware-efficient wavelet-based ECG denoising and R-peak detection architecture for MCT and wearable devices. It is based on a new lifting-based DWT with adapted filters and universal soft thresholding, which effectively removes PLI, MA, and BW noise without loss of essential ECG features. MATLAB simulations validate its effectiveness with improved SNR and reduced MSE. For implementation on FPGA, the design

circumvents multipliers through CSD representation, leading to reduced resource usage and faster processing. With its high operating frequency, the system facilitates real-time low-power processing of ECG signals and is thus best applied in advanced cardiac monitoring systems.

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