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Design of Class F Power Amplifier for Sub 6 GHz

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Abstract

Class F power amplifiers increasingly have widespread use cases in the modern portable mobile communications and higher efficiency operation due to base station. This paper focuses on the design of sub 6 GHz class-F Power Amplifiers (PA) to ensure maximum output power and gain using Gallium nitride– High Electron Mobility Transistor (GaN HEMT). The work also aims to analyze stability and Power Added Efficiency (PAE) using Advanced Design System (ADS) software. Simulations for DC characteristics of the GaN HEMT transistor are performed, stability circles are simulated, and stability factor values have been noted, using ADS software. Stability analysis involves measurements to examine the conditions that may lead to unstable behavior of the PA. The load pull analysis followed by impedance matching is done to transfer maximum power from amplifier stage to load. The input and output network has been designed using transmission lines and incorporated in the final circuit of the PA design. Using the LineCalc tool, the values of electrical parameters are used in the respective MLIN and TLIN circuits, and the respective matching networks are designed at the input side and output side. The amplifier stability factor is 2.276 and the maximum PAE is 65.75%. The maximum output is 39.83 dBm. The layout for the PA network using ADS software has been obtained.

Keywords: Class F power amplifier, GaN, HEMT, Stability analysis, Impedance matching, LineCalc, Input output matching, ADS

1. Introduction

Generally, the main objective of the power amps is to reduce the battery size and power supply consumption. The conventional class – A, B, C, D, E amplifiers provide low efficiency compared to the high efficiency class F power amplifier which has been properly tuned to the

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harmonic components at the output terminals of the transistor device which operates as an ON/OFF switch. The class F power amplifier provides idealistic operation of the collector (or drain) voltage to be shaped as a square wave and the collector (or drain) current to be shaped as a half-wave sinusoidal waveform. It ensures that no overlapping occurs between current and voltage. Hence, in the RF transistor there occurs zero dissipated power and it leads to 100% theoretical efficiency. As the RF device operates as a switch, the collector/drain voltage of the waveforms can be changed by the insertion of multiple harmonic components in the output matching network of the Class F power amplifier.

The class F power amplifier with the help of lumped elements can be used as a switching mode amplifier. In this approach, the expressions for the analysis of the networks are derived in order to evaluate the value of each circuit element in the loading network. But, to match the fundamental frequency, the proper loading network has to be designed. This can also be implemented for all classes of amplifiers by deriving the corresponding equations for the respective conduction angles and operating regions. Hence, the proposed network topology provides a maximum power at the fundamental frequency of 2.4 GHz and the power is reduced at the higher order of harmonics. And this model can be implemented by increasing the operating frequency with careful design of harmonics and matching network.

New communication standards such as 5G and WiFi6/6E have increased the need for RF-Front End Modules. In order to design power amplifiers that satisfy the need for the growing technologies, the design must be such that it reduces transistor loss and increases the practical efficiency using proper design of harmonic resonators by shaping the drain wave forms which leads to less power dissipation. This is the main requirement in many sectors such as in wireless base stations and in modern transmitting chain. Hence, there is a need for the design of power amplifier circuits which provide better efficiency and power outputs compared to the other technologies.

2. Literature Review

Shamil H Hussein et al., [9] designed of a high efficiency class-F power amplifier, with Gallium arsenide material Field Effect Transistor (FET). The class F power amplifier was operated and studied at different operating frequencies. From the results, it was inferred that the amplifier can be operated at input power level more than 15dBm in GSM and CDMA base stations. The design of the class-F PAs were analyzed and studied at an operating frequency of 850 MHz. The technique employed was the load pull technique for the power amplifier

design. The overall procedures such as selecting the DC bias point and analysis, DC bias design simulation, input and output matching network design were discussed in detail. The amplifier has found to produce a good output spectrum at maximum power output level and the 3rd harmonic spectrum is found to be less than the main spectrum by amount of 40dBm or more. Thus, it is inferred that the class F power amplifier has a very good Power Added Efficiency (PAE), gain, and output power at Pout.

K. Husna Hamza and D. Nirmal [3] discussed the solid-state power amplifiers which yield high output power and operate at a very high frequency. To ensure high efficiency, multiple efficiency enhancement techniques like Doherty configuration and envelope tracking techniques were employed. Analysis of efficiency was done with the help of GaN power amplifier. Compared to the conventional GaN power amplifier, the PAE of the GaN Doherty power amplifier has been found to be far higher in efficiency. Thus, it is inferred that these kinds of power amplifiers are a better choice for wireless base transmitters and receivers kind of applications. The reason is that the higher efficiency power amplifier helps to drastically minimize the power wastage at both input and output side. Hence, it reduces the cooling system needs. Linearization techniques like digital pre-distortion were employed in these GaN power amplifiers in order to get a good linearity at high frequencies with good amount of efficiency. GaN material power amplifiers have the potential to develop these high frequency and high power devices. These amplifiers do not get distorted due to its high thermal conductivity. HEMT (High Electron Mobility Transistor) is a kind of FET transistor. This HEMT incorporates a junction layer between the different band gaps of the two materials (i.e., a hetero junction as the channel instead of a doped region, like the way used in MOSFET transistors). This amplifier is found to provide a good amount of efficiency and high efficiency power.

Chatrpol Pakasiri et al., [2] proposed a class-F power amplifier that was modified to operate at a frequency of 433 MHz with medium output power, which was then simulated and implemented. The design process used the following load conditions such as, output impedance of the amplifier is set to operate at the selected frequency, and short and open load operating are at even and odd harmonics. The load measurement was done by Thevinin impedance instead of load pull analysis. To make the model to work as an ideal class F power amplifier, it must be biased. As the load measurements were slightly different from the optimal value, the circuit yielded only a slight increase in efficiency. But when the load condition was pushed more towards class A amplifier, that led to a very low yield in efficiency. Next, the 9 dBm input power and good choice of class AB power amplifier, resulted in 68.5% PAE and 21.8

dBm output power, and an input power 11 dBm circuit generated a very good PAE and output power which was 79.6% with 23.2dBm respectively. This process yielded moderate efficiency. So, this proves to be a better model. But when it is biased near to the class F amplifier, the load value deviated more from load values of load pull analysis.

Md Golam Sadaque et al., [6] suggested a broadband Continuous Class F (CCF) Radio frequency Power Amplifier (RFPA) which is particularly fabricated for the frequency spectrum in the range of 3.3 - 4.3 GigaHertz. The Simplified Real Frequency Technique was employed for designing the matching networks. The "class-F RFPA" is suitable for all the narrowband kind of use cases but it is not much suitable for broadband kind of use cases. The CCF RFPA technique can be easily employed. But there is an issue with the fundamental values and the harmonic values in the current-plane rotation. This issue cannot be solved by matching networks. So, by choosing the optimal value at the current plane, this issue can be solved. It shows that the maximum drain efficiency is 81.5% at 3.5 GHz. The gain was found to be greater than 10 dB over the whole frequency spectrum. The power output yielded was greater than 40 dBm which is appreciable for a power input of 10W device.

Mahya Parnianchi [5] developed a newly fabricated class-F power amplifier, designed method for the input matching, which was then simulated and implemented. An innovative method to design power amplifier (Class F) with a high PAE was presented. The objective of was to provide an improved yield in the output power add efficacy compared to the previous models. The model consisted of a matching network for the input as well as output with low pass filter. The high-efficiency was obtained with the help of low-voltage p-HEMT in the circuit, which was supplied with the optimum DC voltage. It resulted in nth harmonic suppression and hence high PAE was obtained. This result was achieved using the method of analysis of harmonic balance. To validate the model put forth, a PA (class-F) was designed with 1 GHz fundamental-frequency with the help of "ATF-34143 transistor which was used to suppress the unwanted harmonics by introducing the matching networks for the designed fundamental frequency and to minimize the elements parasitic effects. The network proved to provide a high PAE of 80% and Drain Efficiency of 86%, with 12.3 dBm and 2V input power and drain voltage respectively, and more than 28.29dBm was observed as output power. This model of class F power amplifier can be used in modern wireless communications.

The designs of transistors with various methods like low pass matching circuit and harmonic tuning were referred to obtain a PA (class F) having improved efficiency and output power. Tushar Sharma et al., [10] illustrated the time-domain waveform-based analysis in

which both the harmonics of second and third are controlled simultaneously for evaluating the class F power amplifier response. V. Carrubba et al., [1] recommended that both fundamental and second harmonics can be coupled simultaneously for improving the output power and constant and high efficiency. C. Roff et al., [8] explained the methods that are suitable for high efficiency operations of power amplifiers. Liu et al., [4] analysed the methods in which the class-J mode can be used in contrast with class AB power amplifier. But it should not require any additional circuitry, so that the model will serve as a simplified model without the need of matching networks. Pedro et al., [7] elaborated the Cripps load-line method which is a very useful method to find the load pull contours, and estimated the efficiency of those contours.

Based on the above literature survey, it has been observed that Gallium nitride (GaN) HEMT showed improved features, and class F power amplifier design with an antenna is found to be better. In comparison to other amplifiers, switching amplifiers like class F yield better efficiency and output power. Hence, this work employs power amplifier (class F) design with suitable optimizations to yield the desired output power and efficiency.

3. System Design Process

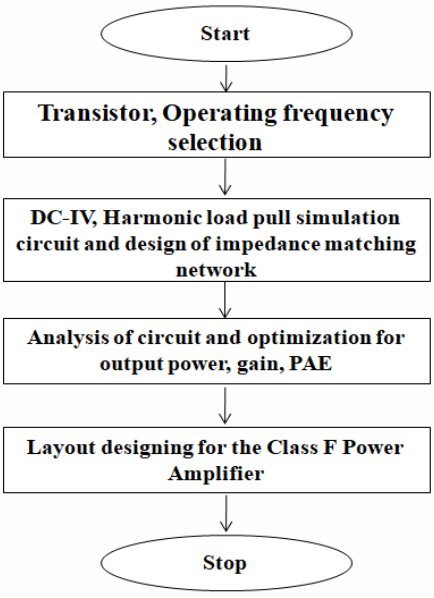


Figure 3.1 Flow diagram of power amplifier design

The initial step is to choose the suitable transistor for the implementation of the amplifier and to decide the operating frequency for which the amplifier has to be implemented.

The frequency chosen is sub-6GHz (i.e.,) 2.4 GHz and the transistor is GaN HEMT as it has high frequency ranges.

Once the transistor is chosen, the DC-IV characteristic and bias point (stability) is analyzed to obtain the operating point values for the transistor. In stability analysis, the stability of the transistor for that particular frequency is viewed and verified. The stability is verified based on the condition that the Rollet's stability factor (K factor) has to be greater than or equal to1. If the condition is not satisfied, then the system will have oscillations. The next step is load-pull simulations and the design of an impedance-matching network. The load and source impedance values which are obtained from the datasheet for the desired frequency are used for load-pull analysis to get maximum PAE and desired output power. From the load-pull analysis, a set of load and source impedances are obtained by adding and varying the resistance to yield the best choice of load source impedance.

The impedance matching network is designed using the obtained load and source impedance values from load-pull analysis. This is done in order to minimize signal reflection and maximize the power transfer. The next step is input and output matching network design. For this step, there involves two separate networks. The output matching network is designed first, then it is followed by the designing of input matching network. The impedance matching is done either using a harmonic matching network or smith chart analysis. The improper matching leads to power loss, signal reflection and also affects the gain, performance, and efficiency of the amplifier. The circuit is then analyzed to observe the gain and the output power. The next step is to optimize the power amplifier for fundamental and harmonic performance.

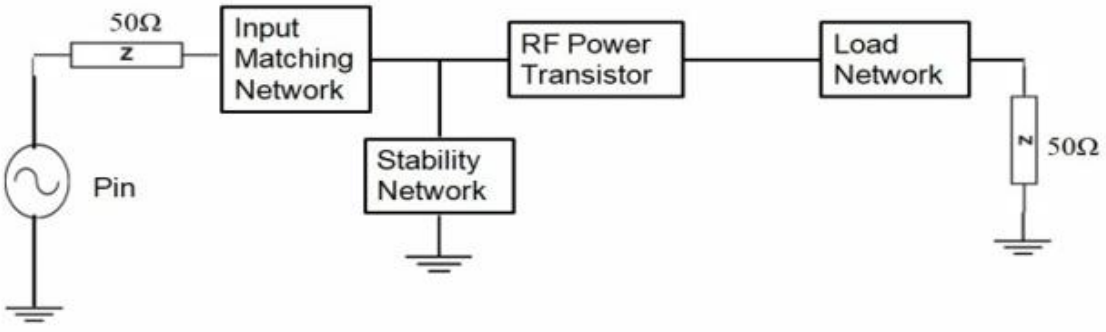


Figure 3.2 Block diagram of Linear Power amplifier

The proposed block diagram in Fig. 3.2 represents the overall circuit of the linear power amplifier. Here, the transistor used is GaN HEMT. The GaN HEMT transistor provides high power density, high breakdown voltage, and reduces power requirements. The stability network is to maintain the stability of the amplifier and to prevent oscillations. The voltages are obtained from DC-IV bias point analysis. The matching of source and load impedances is done which are obtained from the load-pull analysis. Those impedances are connected to the circuit. Harmonic balancing is performed to identify the power levels available at various harmonic frequencies. This is done in order to suppress the higher – order harmonics and have fundamental frequency (operating frequency) alone.

4. System Design

4.1 DC Characteristic Analysis

Biasing a transistor is the process by which the transistor's DC operating voltage or current conditions is set to a correct level so that any AC input signal can be amplified appropriately by the transistor. The device, CGH40010F transistor has been taken from the Cree's library. This device is gallium nitride -high electron mobility transistor. The DC characteristics of the CGH40010F transistor is analyzed, and also the drain current and the drain voltage are found from the simulation of the biasing network. The gate bias is set between -2 to -4 V and the drain bias is from 0 to 70 V, but this device works only at 28 V. The reason for choosing 70 volts is that, the drain voltage must always be more than twice that of operating voltage.

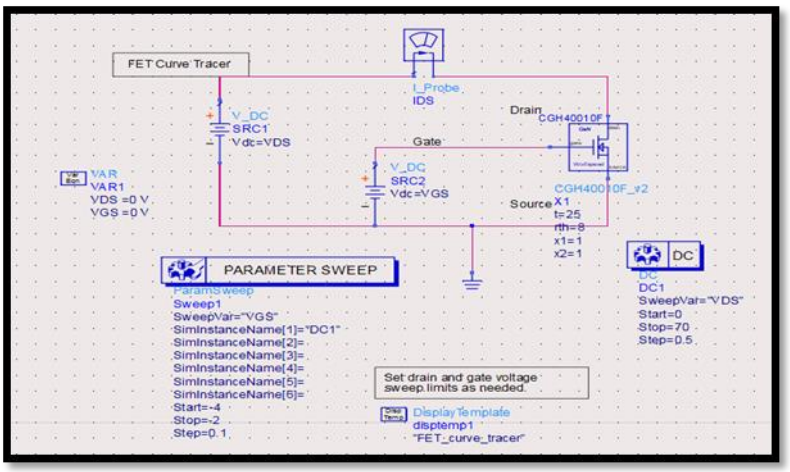


Figure 4.1 DC and bias point analysis circuit

The FET tracer curve template in ADS is used for load line analysis and determining the Q-point (bias point). Fig. 4.1 shows the circuit of DC characteristic analysis in ADS.

4.2 Stability Analysis

Stabilization is the process of making the operating point independent of temperature changes or variations in the parameters. The stability analysis in ADS is done using the network analyzer, SP_NWA available in simulation instruments library. Stabilization must be achieved for the reasons given below.

- Temperature dependence
- Thermal runaway
- Variations in Q-point

The same bias of -2.7 V to 28 Volt is set, which was used for DC characteristics analysis. And the operating frequency is set to be around 0.5 GHz to 6 GHz. For displaying the stability circles, S parameters, the preconfigured data display templates are used. The Rollet's stability factor is represented using Equation [1]. Using Equation [1], the K-factor (Stability Factor) of a RF Amplifier is calculated from the S parameters (S11, S12, S21 and S22).

$$k = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + \Delta^2}{2|s_{12}||s_{21}|} \tag{1}$$

where,

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{2}$$

When Rollet's factor > 1, the RF power amplifier is said to be unconditionally stable.

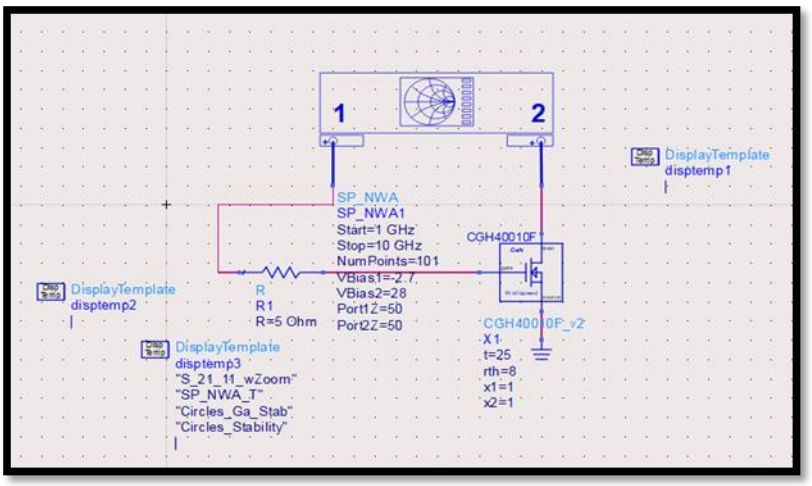


Figure 4.2 Stability analysis circuit

Stability analysis of the GaN HEMT is done and the corresponding Rollet's Stability Factor K is noted for different frequencies by performing a frequency sweep, and it is observed that the K-factor is less than 1 for the operating frequency 2.4GHz. If the stability factor is less than 1, it shows that the transistor will be unstable for the particular operating frequency and there will be oscillations. Hence, a resistor of 5 Ohms is added to make the transistor stable. Fig. 4.2 shows the SP_NWA network that has been simulated.

4.3 Load-Pull Analysis

Load-pull varies the impedance systematically for a transistors /DUT (device under test), to access its power counters and PAE counters, and the related settings for providing a better network performance. Fig. 4.3 shows the load-pull analysis carried out in ADS. The load-pull simulation tool is obtained from the design guide (constant available source power present in the one tone load-pull simulations of the load-pull). The stabilized device is connected and the finalized DC bias and the RF frequency is set to 2400 MHz. For the input power of 29 dBm, from the design and simulation, the output power of 40 dBm is achieved. And the fundamental Zload is kept at 20 Ohm and Zsource is kept at 5 Ohm. The second and third harmonic of the load can be either open or short circuited when analysing the fundamental performance. By varying the impedance of the source port, source-pull simulation is done. The biasing voltages are obtained from the DC analysis. A set of power contours, usually on a smith chart is mapped; this is used to determine the maximum power output that can be achieved for a given load. These contours are of great use in calculating the actual impedance of the device when it is being used.

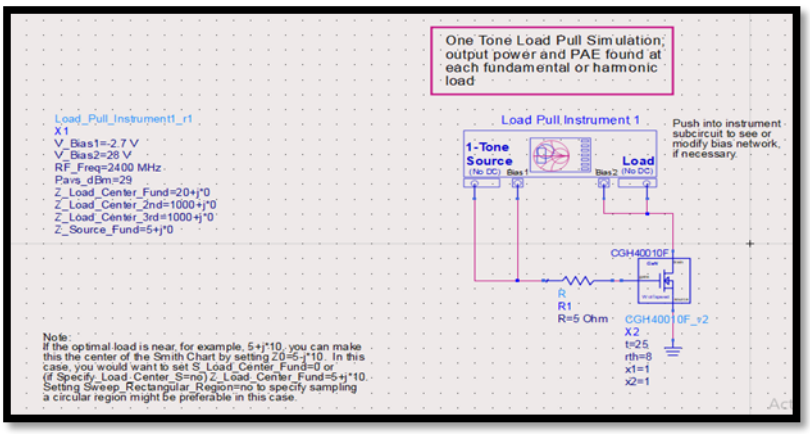


Figure 4.3 Load-pull analysis circuit

4.4 Matching Network (Input and Output)

The source and the load impedance values obtained from load-pull simulation are used in the impedance matching requirement circuit. To synthesize the matching network, there are two utilities available in ADS: Smith chart utility and Impedance matching utility. The input and output matching circuits in Fig. 4.4.a and Fig. 4.4.b are designed using physical micro strip lines (MLIN Substrate). The smith chart component is placed in the schematic workspace and the input and output terminal of the component are the source and the load impedances respectively. The values for source and load impedances values from the load-pull analysis are set and the given values are locked in the smith chart utility.

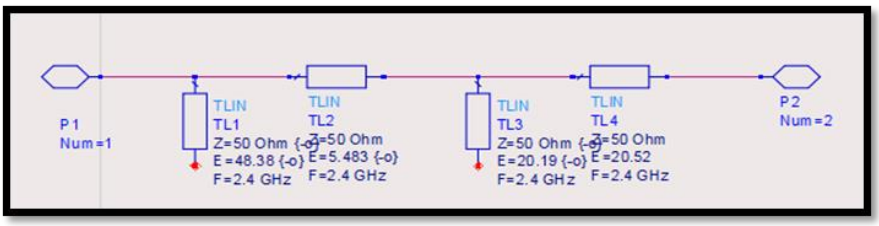


Figure 4.4.a Input matching network

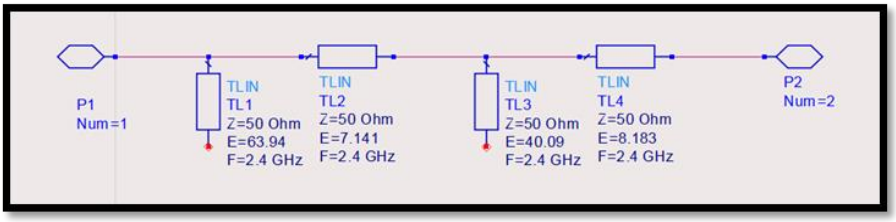


Figure 4.4.b Output matching network

Every component in the utility such as series inductor, parallel inductor, series capacitor, micro strip stub, etc. has different trajectories. They are used on the basis of trial and error method to design the network. Simultaneously the network response is noted for the specified range of frequencies. When the circuit is simulated for S parameters, the resonance match at the operating frequency is noted. When lumped elements are used in the network, it might affect the quality of the network and may lead to practical losses because of their low Q factor. Therefore, the typical Q factor value is entered in the utility and the trajectory is now changed. The equivalent transmission line circuit is designed and it is copied to a new workspace to convert the transmission line circuit to physical micro strip lines.

In ADS, the LineCalc utility is available where electrical and physical values of various transmission lines can be calculated. In the LineCalc tab, the physical parameters are fed and analyzed to calculate the electrical parameters. When the electrical parameters are synthesized, the physical parameters are computed and used in the network to obtain the desired network. The MLIN circuit is obtained, and this final network is used in the impedance matching network design. The circuit is later optimized for better performance and the network response is analyzed. The circuit in Fig. 4.5 represents the final power amplifier circuit. The harmonic analysis and optimization has been done and the final circuit is generated as layout. The smith chart in the circuit can be pushed in, to view the transmission line circuit.

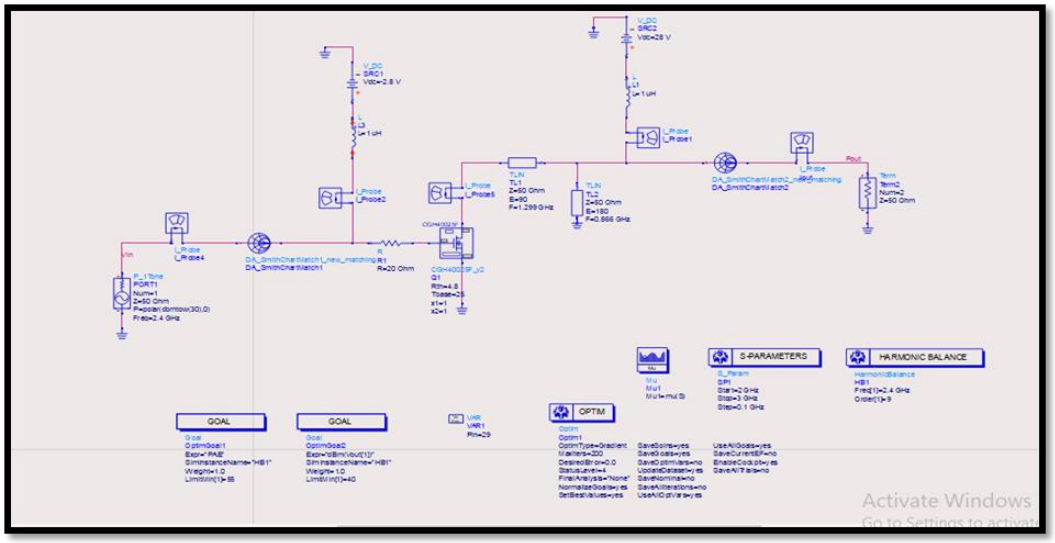


Figure 4.5 Final Power Amplifier Circuit

5. Results and Discussion

5.1 DC Characteristics Analysis

The results of DC Characteristics and the bias point analysis are shown in Fig.5.1. Ids vs Vds is plotted and the corresponding load-line is obtained. The load-line is plotted by adding the slope equations in the output window. The values are displayed by placing a marker on the plot. The marker is placed in order to obtain the biasing voltage for class F operation. The obtained values have also been verified using data sheet. The operating region for the class F amplifier is the active region. The biasing voltage is set to 28 V and -2.7 V (from the datasheet in the reference [11]) to obtain a large signal gain and high efficiency from the DC analysis.

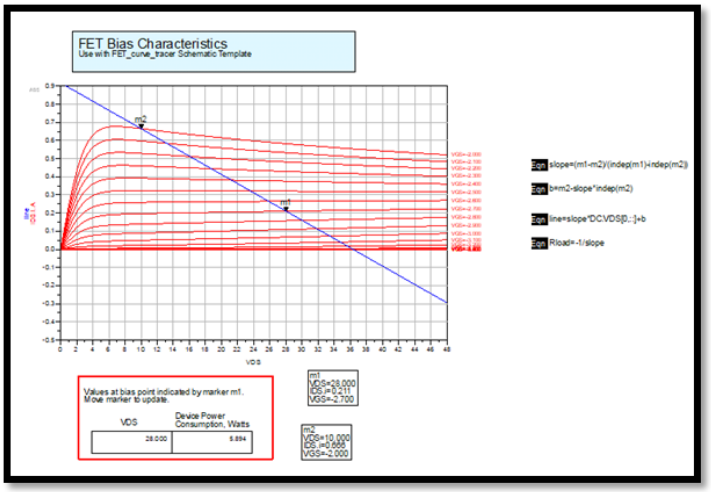


Figure 5.1 DC I-V and bias point analysis

5.2 Stability Analysis

The results of the stability analysis are shown below. The Rollet's stability factor obtained in Fig. 5.2.a is 2.276 which satisfies the stability condition (stability factor should be greater than 1). Hence the system is unconditionally stable. i.e., the possibility of oscillations are avoided.

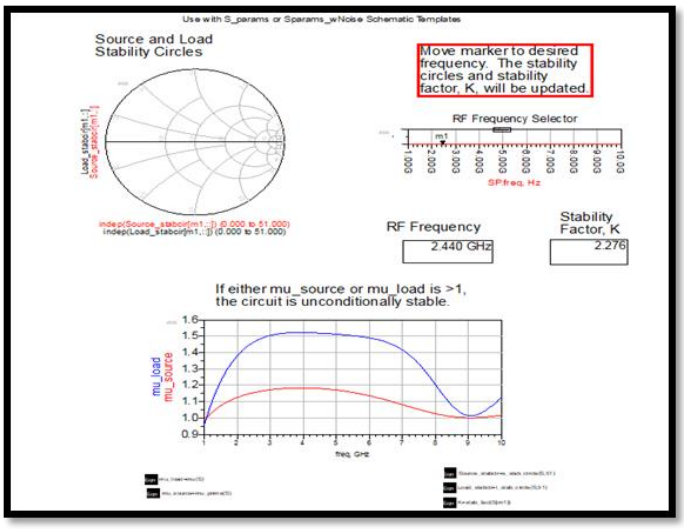


Figure 5.2.a Stability curves

It is also observed that the load and source circles are out of the smith chart (around the frequency of 2.4 GHz), and the system is unconditionally stable. The 5 Ohm resistor not only increases stability but is also concerned with the amount by which the gain is dropped.

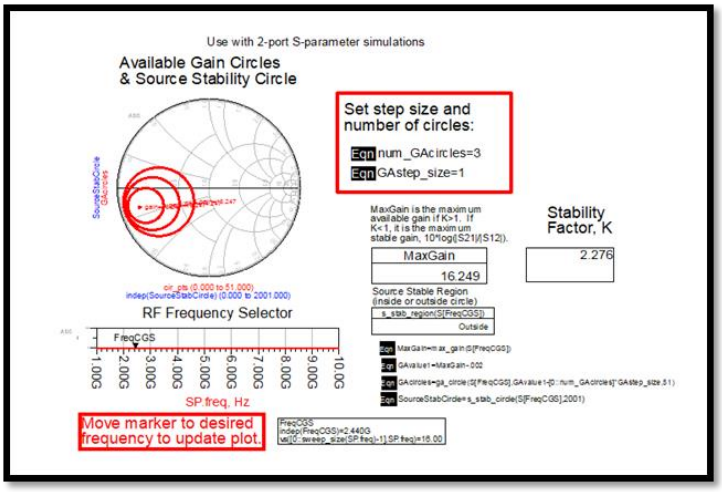


Figure 5.2.b Circles_Ga_Stub

Fig. 5.2.b shows the available gain circle and source stability circles of the Ga stub. It is also found from the figure that the source stable region is outside the circle which is necessary for a PA to be stable. Fig. 5.2.c shows the stability parameters obtained after stability analysis. These values are found to be accurate once the impedance matching is done, and the gain will be increased as per the requirement.

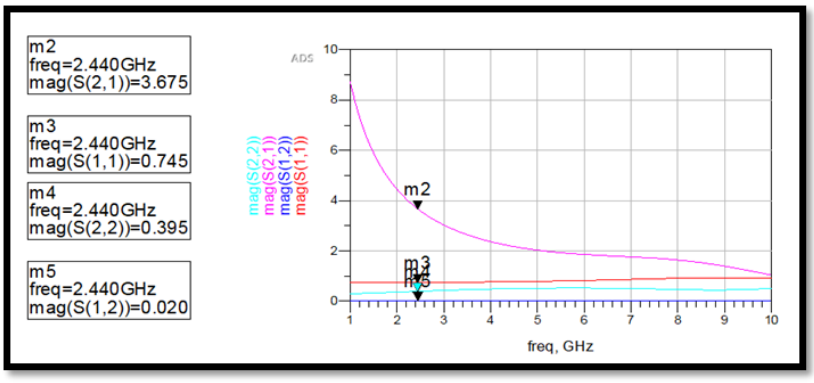


Figure 5.2.c Network analysis – Stability parameters

5.3 Load-Pull Analysis

Load-pull analysis gives the useful insights for impedance matching at the input and output. Fig. 5.3.a and fig. 5.3.b show the results of load-pull analysis. This is used to construct the set of contours which determines the maximum power output, PAE, and the power contour levels achievable with a given load impedance. Fig. 5.4.a and fig. 5.4.b show the power contours, PAE contours, and gain contours. The maximum power obtained is 41.589 dBm and maximum PAE obtained is 65.759%.

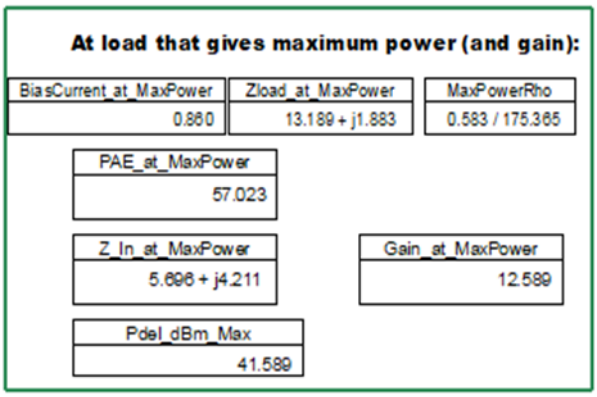


Figure 5.3.a Load at maximum power

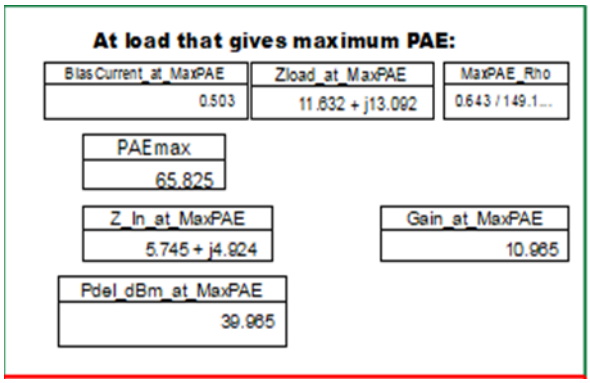


Figure 5.3.b Load at maximum PAE

Fig. 5.3.a represents the values of source and load impedances which can be used to obtain maximum power, and it is found to be 5.696+j4.211Ω and 13.189 +j1.883Ω respectively. Fig. 5.3.b represents the load and source impedance values for maximum PAE requirements. Fig. 5.4.a shows the power and PAE contours and fig. 5.4.b shows the gain contours.

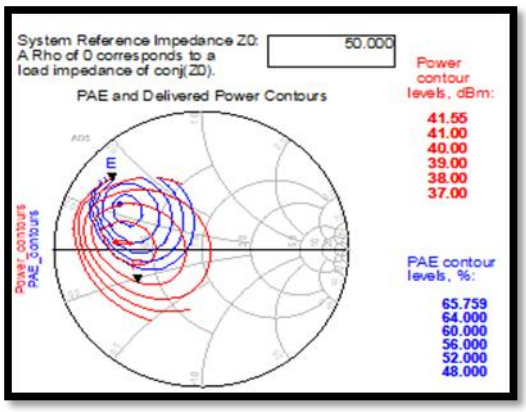


Figure 5.4.a Power and PAE contours

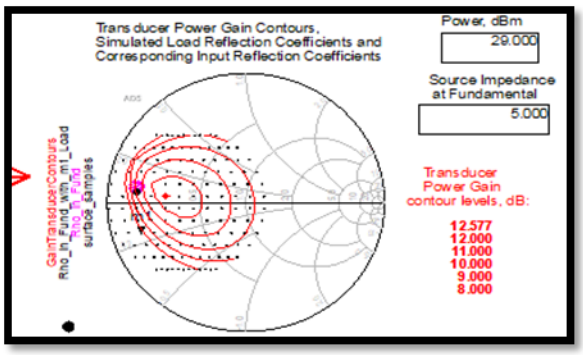


Figure 5.4.b Gain contours

5.4 Input and Output Matching Network

Fig. 5.5.a shows the result of the input matching network response and fig. 5.5.b shows the result of the output matching network response.

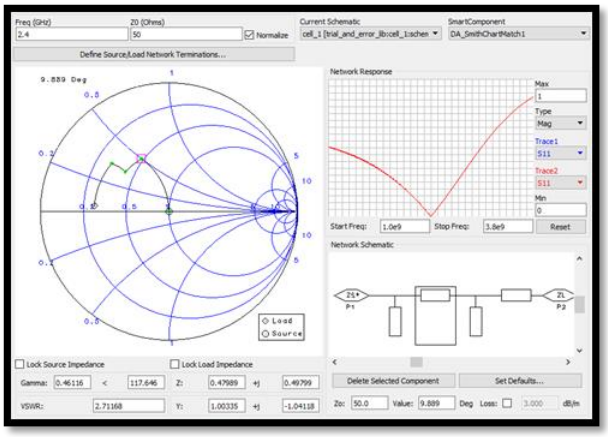


Figure 5.5.a Input matching network response

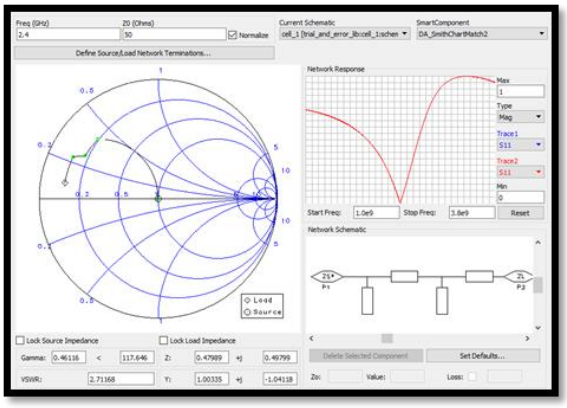


Figure 5.5.b Output matching network response

Here, the results are obtained using a technique where except for fundamental frequency all other harmonics are short-circuited. The output impedance observed in load-pull analysis is matched using transmission lines. Fig. 6.6 shows the result obtained for matching network in the input and the output. It can be seen that at the fundamental frequency, a maximum output power of 39.83 dBm has been obtained.

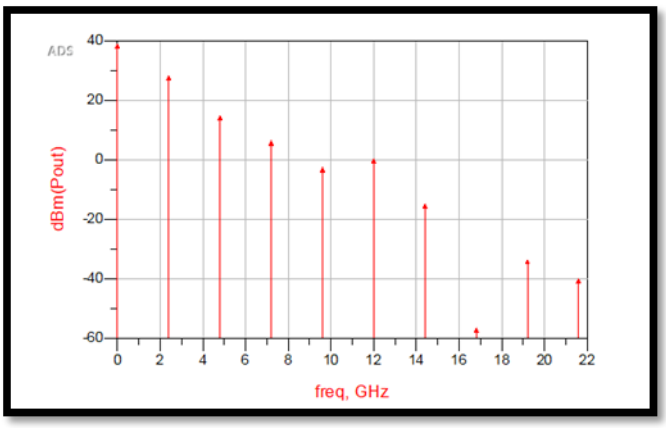
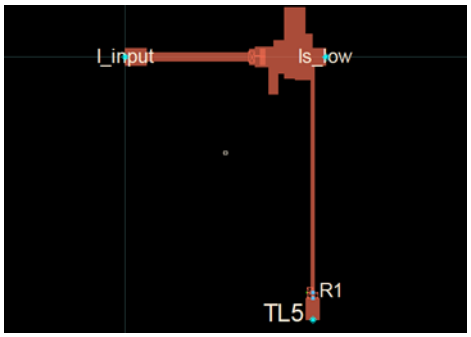


Figure 5.6 Input and output matching network graph

6. Layout Design

The layout for the matched input and output impedances is obtained. The transmission lines are replaced with the substrate to obtain the layout. The layout is obtained by connecting the input-output matching circuit. Fig. 6.1 shows the final layout design.



7. Conclusion and Future Work

The class F linear power amplifier which has been designed using ADS software for sub-6 GHz shown in this research, has achieved around 65.75 % PAE with acceptable linearity. The simulated results infers that the GaN HEMT linear power amplifier is found to be stable for a wide range of frequency spectrum and offers high gain with high switching speed. A class F amplifier with a center frequency of 2.4 GHz has been designed and simulated using a GaN HEMT transistor. The power amplifier shows a maximum power added efficiency of 65.75%. The maximum output obtained is 39.83 dBm. The amplifier stability factor obtained is 2.276. The load and source impedance values obtained are 5.696+j4.211Ω and 13.189+j1.883Ω. The future work is to fabricate the class F power amplifier that is designed using ADS software and perform real-time testing with GaN HEMT transistor for a frequency of 2.4 GHz.

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