Journal of Electronics and Informatics (ISSN: 2582-3825)
www.irojournals.com/iroei/

The Power Optimization and an Area Efficient of Static RAM 1-Bit Cell using CMOS Novel Technologies

Gaje Sahruday[1], Anumula Srikanth[2], Karne Harikrishna[3]

Department of Electronics and Communication Engineering, Vaagdevi Engineering College
Bollikunta, Warangal, Telangana 506002, India.

E-mail: [1]sahruday.gaje@gmail.com, [2]anumulasrikanth1212@gmail.com, [3]karneharikrishna66@gmail.com

Abstract

In order to meet all the expectations of consumers, today's technology is all equipped with large capacity memories. Additional factors include power consumption and delay, all of which are crucial in determining how well a gadget performs. Memory is an important factor of many widgets, and as devices get smaller, their size likewise gets less. Every computerized device, as a result, uses little power, and speed is of utmost importance. Since 6T Static Random Access Memory (SRAM) cells have advantages over other cells, the current scenario suggests that they are frequently employed for SRAM-based memory systems. Today's electronics businesses are primarily concerned with minimizing power consumption, with static and dynamic power dissipation being the two key considerations. Meeting customer demands, high bandwidth, low power, and fast-consuming storages are also required. The major objective of this research is to decrease the power dissipation of the SRAM. The main problem faced by the digital industry is the decrease of power and delay. By connecting two Complementary MOSFET inverters back-to-back, an SRAM cell can be set up in an easy and beneficial manner. This setup offers good noise immunity.

Keywords: Static Random Access Memory (SRAM), Low Power Consumption and Delay

1. Introduction

In order to produce high-speed logic gates for digital circuits with minimal power dissipation [1], Complementary MOSFET (CMOS) technology was developed [2]. CMOS enables the creation of multiple powerful analogue and digital circuit designs. Although no current flows into the gate of a CMOS, it is similar to BJT logic devices in that it switches by voltage rather than current. In the 1970s, CMOS technology was limited to specific consumer

DOI: https://doi.org/10.36548/jei.2023.2.001
Received: 28.03.2023, received in revised form: 28.04.2023, accepted: 13.05.2023, published: 23.05.2023

sectors, including electronic watches. The VLSI technology did, however, shift to CMOS in the 1980s as a result of benefits including low power consumption, high noise margin, a broader temperature and voltage operating range, overall circuit simplification, an electro migration problem, dependability, and layout ease. Millions of transistors were integrated onto a single chip with the development of VLSI in the 1980s. For VLSI digital and mixed-signal designs right now, CMOS is the dominant technology [3]. Compared to transistor-transistor logic, CMOS is faster, more suited to working at low supply voltages, and uses less power. The N-type and P-type semiconductors that are present in each transistor are referred to as the "complementary" parts of CMOS. More electrons than holes, or locations where an electron may be, are present in N-type semiconductors. In comparison to electrons, holes are more abundant in P-type semiconductors. Depending on how the circuit is built, these two semiconductors may cooperate to generate logic gates.

Since the invention of CMOS in 1959, Static Random-Access Memory (SRAM) has been the primary driving force behind every new CMOS-based technology fabrication method. A hard-wired memory cell was developed in 1965 by IBM employees Arnold Farber and Eugene Schlig, utilising a transistor gate and tunnel diode latch. The Farber-Schlig cell is the result of their decision to replace the latch with two transistors and two resistors. A 16-bit silicon memory chip based on the Farber- Schlig cell was developed in 1965 by IBM's Benjamin Agusta and his team. It contained 80 transistors, 6 resistors, and 4 diodes. SRAM is a type of RAM that stores each bit using latching circuitry (flip-flops). Data is lost when the power is interrupted since SRAM is a volatile type of memory. The adjective "static" distinguishes SRAM from Dynamic Random-Access Memory (DRAM), which requires frequent updates. While DRAM is utilised for a computer's primary memory, SRAM is mostly employed for a CPU's cache and internal registers. SRAM outperforms DRAM in terms of speed and cost [4].

Bit line toggling of the SRAM system during write operation causes the greatest amount of power dissipation. A new SRAM architecture that incorporates charge pump circuits to recycle the bit line charge is suggested to lessen this level of power loss [5-6]. Following the simulation, an 11% power reduction and a 3.8% area overhead reduction are made. The major goal of this research is to evaluate the performance of present 6T CMOS SRAM well in 45nm and 180nm technologies in terms of power consumption, latency, and SNM [7-8].

The traditional 6T SRAM cell is modified in this research with a sensing amplifier, improving the differential voltage of the bit lines. The use of differential bit lines is due to

common mode rejection. As a result, the impact of noise and signal degradation can be reduced. Using the Cadence tool, the modified 6T SRAM cell is examined under various power supply and temperature conditions [9]. Power loss includes a significant portion of leakage current. Here, some methods for reducing leakage current are suggested. In standby state, leakage current plays a significant role. The power consumption of CMOS transistors is caused by various parameters. Deep sub-micron techniques can be used to reduce process leakage current.

Research [10] presents a 45-nm CMOS device that suppresses reference sidebands to less than -65 dBc while drawing only 4 mW from the power supply. A Fractional-N loop has also been successfully added to the wideband architecture. It has low noise levels, lower chip size, but designing is challenging. Research [11] provides a power demand and in-band phase noise of 112 dB, that is adequate for wireless communication applications. It offers a 2.95 second lock time. The design's use of 180nm CMOS technology is a disadvantage [12].

2. Existing Method

A. Objective

The main objective is the designing of the 180nm, 90nm, and 45nm CMOS-based 6T SRAM. For each 6T SRAM cell in this manner, the delay analysis and power dissipation in 180nm, 90nm, and 45nm technology have been computed. The same process is applied in 32nm and 22nm in the provided approach because power consumption and latency are a bit excessive.

B. 6T SRAM Design In 180nm

In the design of SRAM cache memory, the 6T bit-cell is the frequently utilized industrial standard bit cell. It is advised to be familiar with the read and write operations of the 6T bit-cell in order to fully understand the layout design.

One can build the smallest bit cell unit that contributes to the total SRAM memory area on the device by choosing the widths of the six transistors in the 6T bit-cell with prior knowledge of read/write operations. The 6T bit-cell read operation is shown in Figure 1 while its write operation is shown in Figure 2.

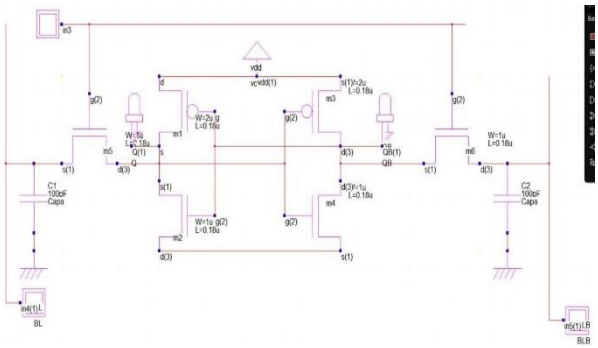

Figure 1. Schematic Diagram of 6T SRAM Cell Design in 180nm (READ)

C. Circuit Operation

The in side part is called the memory part, and to the memory part, 2 inverters are connected. The working of NOT gate and CMOS inverters are the same.

SRAM consists of Bit Line (BL) and Bit Line Bar (BLB) for accessing the circuits. If Word Line, WL=1, BL and BLB can be accessed and both are in ON condition and also WL=1 can be done in READ and WRITE operations. If WL=0, the circuit accessing is lost and it is in HOLD operation.

BL and BLB are used as input lines for write operation in circuit, whereas BL and BLB are used as output lines for read operation in circuit. The circuit consists of pre-charged capacitors which are used for READ and WRITE operations. The above circuit is designed with 180nm transistors, 4x180nm NMOS transistors and 2x180nm PMOS transistors, and they are denoted as M1, M2, M3, M4, M5, and M6. Here M1, M2, M3, and M4 form pairs of internal inverters which are used to store information. M5 and M6 are called accessing transistors used to access the inverter pairs for READ and WRITE operations. 180nm, 90nm, and 45nm numbers represent the minimum feature size of the transistor (PMOS or NMOS). The smaller the size, the larger the number of transistors can be fabricated on the chip, as the above circuit is designed with 180nm.

D. Read Operation

Memory should hold some value that must be Q=1 and QB=0. To read, BL and BLB should be used and WL=1 is made, then the access transistors will be in ON condition. The memory must be read, so it must be made sure that BL and BLB (input or output) must be in output lines.

At pre-charge capacitors, the voltage should be VDD. There is a voltage difference between nodes. When Q=1and VDD=1, there is no voltage difference and the capacitors will not discharge.

When QB=0 and VDD=1, there is a voltage difference and the capacitors will discharge,and the current will flow. As node voltage decreases, the BLB decreases and voltage decreases.

Now the values must be sent to BL and BLB to the sense amplifiers. They act as comparators and will notify that if the BLB value decreases, then the output should be 1. Hence, one can read successfully into the memory.

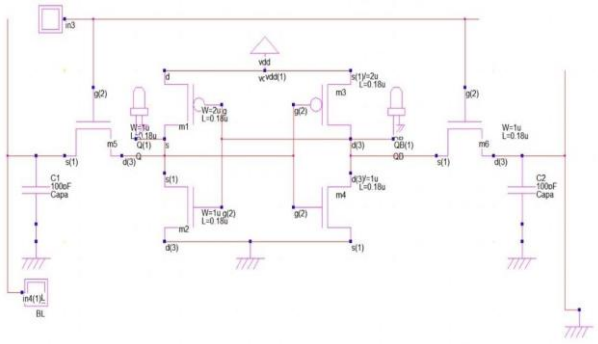

Figure 2. Schematic Diagram of 6T SRAM Cell Design in 180nm (WRITE)

E. Write Operation

In order to do write operations, the memory bit musthave Q=0, QB=1, and WL=1. First, the BLB is connected toground since the BL must be controlled. By altering the transistors aspect ratio, M4 can be made stronger than M3and the voltage difference between Q and BLB needed to write 1 into the SRAM cell can be achieved.

Hence, after the operation, Q becomes 1 instead of Q=0, hence one can successfully write to the memory.

F. Hold Operation

This is the state when the SRAM cell is idle and the BL and BLB (data path) are kept at ground when the access transistors are disconnected because the WL is not connected.

If the WL=0, then the circuit accessing is lost and it is in hold operation.

3. Results and Outcomes of the Existing Method

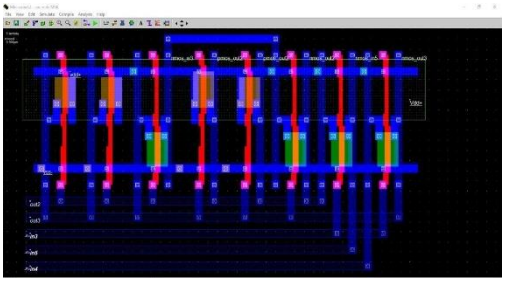

Figure 3. Microwind Simulation of 6T SRAM (180nm) READ

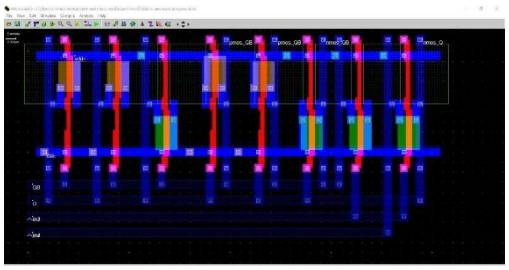

Figure 4. Microwind Simulation of 6T SRAM (180nm) WRITE

4. Simulation Results of the Existing Method

A. Read

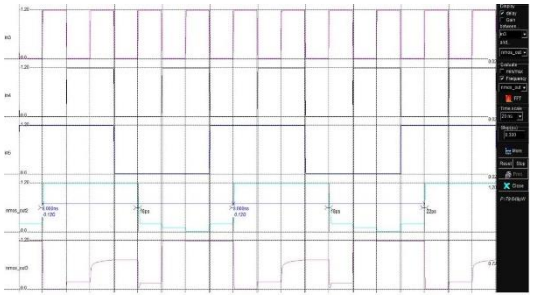

Figure 5. Delay Analysis of 6T SRAM (180nm) During READ

As shown in figure 5, the delay is calculated from the simulation. As it is observed that the rising time is 1016ps and the falling time is 1022ps, the total delay is obtained in read operation.

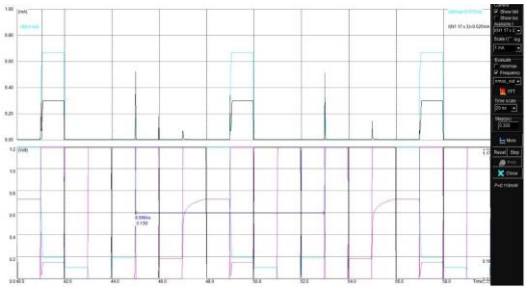

Figure 6. Power Analysis of 6T SRAM (180nm) During READ

As shown in figure 6, thestatic power and dynamic power in 6T SRAM are calculated from the simulation. It is observed that the static power is 119µm and the dynamic power is 482.4µm in the read operation.

B. Write

As shown in figure 7, the delay is calculated from the simulation. As it is observed that the rising time is 1024ps and the falling time is 1018ps, the total delay in write operation is obtained. As shown in figure 8, the static power and dynamic power in 6T SRAM are calculated from the simulation. It is observed that the static power is 129µm and the dynamic power is 377.28µm in the write operation.

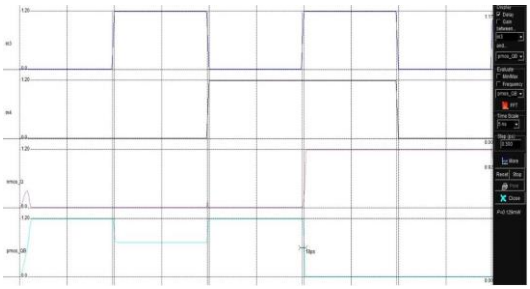

Figure 7. Delay Analysis of 6T SRAM (180nm) During WRITE

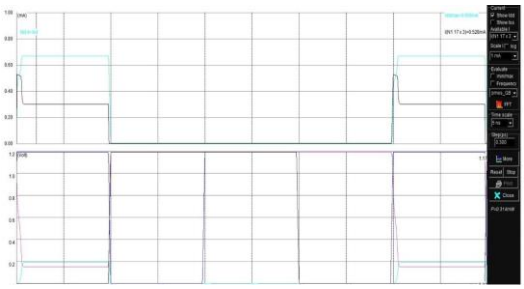

Figure 8. Power Analysis of 6T SRAM (180nm) During WRITE

5. Calculations of the Existing Method

A. At 180nm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 180nm =

Width*Length of PMOS+ Width*Length of NMOS

= 2µm*2*0.18µm+1µm*4*0.18µm

= 1440nm^2

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 180nm = (1016+1022)/2

= 1019ps

Static Power:

Static power in 180nm = 119µm (read operation)

Static power in 180nm = 129µm (write operation)

Dynamic Power:

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 180nm = 482.4µw (read operation)

Dynamic power in 180nm = 377.28µw (write operation)

B. At 90nm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 90nm =

Width*Length of PMOS+ Width*Length of NMOS

= 2µm*2*0.09µm+1µm*4*0.09µm

= 720nm^2

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 90nm = 1016ps

Static Power:

Static power in 90nm = 111µm (read operation)

Static power in 90nm = 181µm (write operation)

Dynamic Power:

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 90nm = 501µw (read operation)

Dynamic power in 90nm = 438.48µw (write operation)

C. At 45nm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 45nm =

Width*Length of PMOS+ Width*Length of NMOS

= 2µm*2*0.045µm+1µm*4*0.045µm

= 360nm^2

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 45nm= 1017ps

Static Power:

Static power in 45nm = 110µm (read operation)

Static power in 45nm = 179µm (write operation)

Dynamic Power:

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 45nm = 502µw (read operation)

Dynamic power in 45nm = 438.48µw (write operation)

6. Research And Outcomes of the Existing Method

The below table contains the data collected from the simulation of a 6T SRAM cell by using 180nm, 90nm, and 45nm CMOS technology. In the below table, the width of the PMOS and NMOS are constant and length of the gate is changed and the below values of READ and WRITE operations are obtained. The total delay and area are also obtained.

Table 1. Existing Method Values of Power, Area, and Delay.

Type of SRAM	Variable width of Nmos µm	Width of Pmos µm	Variable length of gate	Read		Write		Total delay ps	Area nm2
				Operation µW					
				Ps	Pd	Ps	Pd		
6T	1	2	180nm	119	482.4	129	377.2	1019	1440
6T	1	2	90nm	111	501	181	438.4	1016	720
6T	1	2	45nm	110	502	179	438.4	1017	360

7. Proposed Method

The main objective of the proposed method is the designing of 6T SRAM using 32nm and 22nm CMOS technology. In this method, delay and power dissipation for each 6T SRAM cell are analyzed. The critical voltage and transistor ratio are the key factors in the delay in 32nm and 22nm. Using various methods will reduce power dissipation. One of the most popular techniques for achieving low power dissipation is low power supply voltage (VDD). SRAM's battery life is improved when low supply voltage is applied. In view of this, the 6T SRAM cell's delay and power consumption are analyzed and calculated using CMOS technology. Design of 32nm 6T SRAM cell is depicted in Figure 9 (READ) and Figure 10 (WRITE)

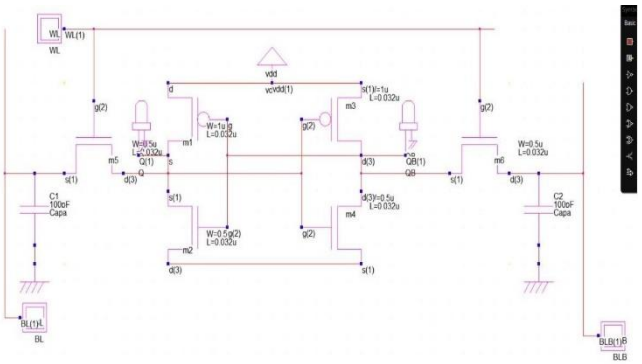

Figure 9. Schematic Diagram of 6T SRAM Cell in 32nm (READ)

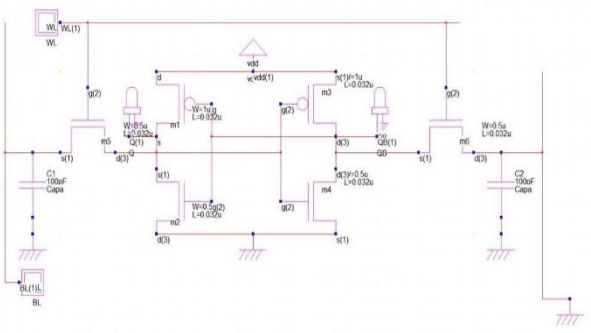

Figure 10. Schematic Diagram of 6T SRAM Cell in 32nm (WRITE)

8. Results and Outcomes of the Proposed Method

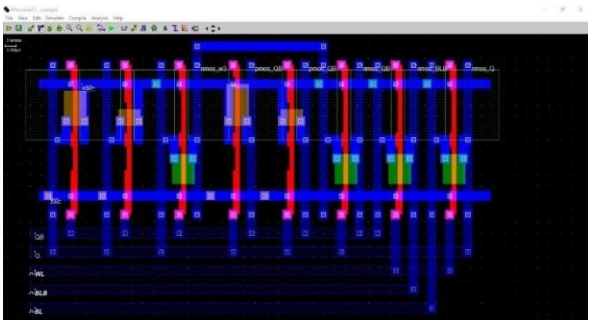

Figure 11. Microwind Simulation of 6T SRAM (32nm) READ

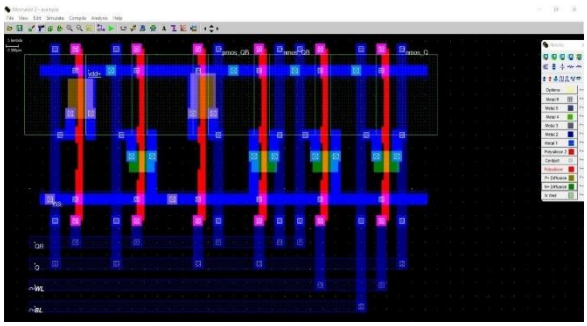

Figure 12. Micowind Simulation of 6T SRAM (32nm) WRITE

9. Simulation Results of the Proposed Method

A. Read

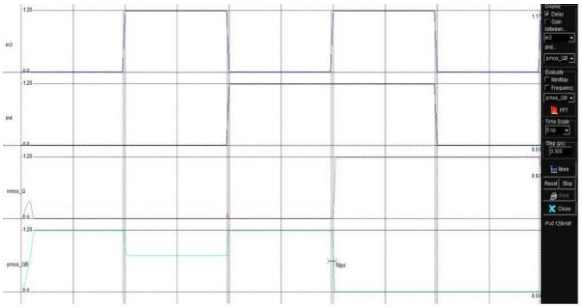

Figure 13. Delay Analysis of 6T SRAM (32nm) During READ

As shown in figure 13, the delay is calculated from the simulation. As the rising time is 1016ps and the falling time is 1011ps, the total delay in read operation, when the width is 1um, is obtained. As shown in figure 14, the static power and dynamic power in 6T SRAM is calculated from the simulation. It is observed that the static power is 53.247µm and the dynamic power is 208µm in write operation, when the width is 1µm.

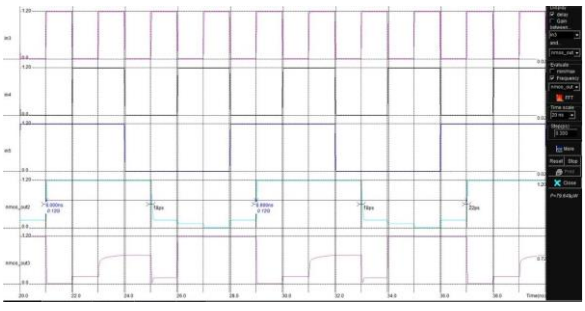

Figure 14. Power Analysis of 6T SRAM (32nm) During READ

B. Write

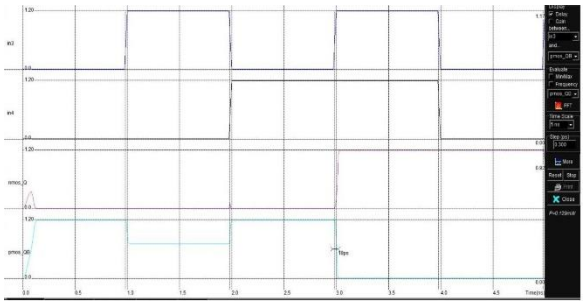

Figure 15. Delay Analysis of 6T SRAM (32nm) During WRITE

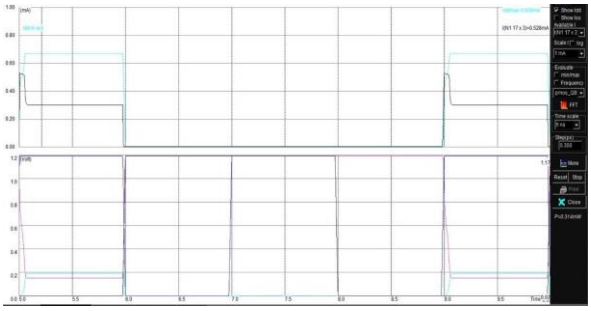

Figure 16. Power Analysis of 6T SRAM (32nm) During WRITE

As shown in figure 15, the delay is calculated from the simulation. As the rising time is 1016ps and falling time is 1022ps, the total delay in read operation, when the width is 1um, is obtained. As shown in figure 16, the static power and dynamic power in 6T SRAM are calculated from the simulation. It is observed that the static power is 137µm and dynamic power is 193.59µm in write operation, when the width is 1µm.

10. Calculations of The Proposed Method

A. At 32nm

Stage 1: width = 2µm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 32nm =

Width*Length of PMOS+ Width*Length of NMOS

= 2µm*2*0.032µm+1µm*4*0.032µm

$= 256nm^2$

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 32nm= 1011.5ps

Static Power and Dynamic Power can be calculated as:

Static power in 32nm = 53.247µm (read operation)

Static power in 32nm = 137µm (write operation)

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 32nm = 208µw (read operation)

Dynamic power in 32nm = 193.59µw (write operation)

Stage 2: width = 1.5µm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 32 nm =

Width*Length of PMOS+ Width*Length of NMOS

$= 1.5µm*2*0.032µm+0.75µm*4*0.032µm$

$= 192nm^2$

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 32nm= 1018ps

Static Power and Dynamic Power can be calculated as:

Static power in 32nm = 84.32µm (read operation)

Static power in 32nm = 68.646µm (write operation)

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 32nm = 217µw (read operation)

Dynamic power in 32nm = 95.175µw (write operation)

Stage 3: width = 1µm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 32nm =

Width*Length of PMOS+ Width*Length of NMOS

= 1µm*2*0.032µm+0.5µm*4*0.032µm

= $128nm^2$

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 32nm= 1517.5ps

Static Power and Dynamic Power can be calculated as:

Static power in 32nm = 41.302µm (read operation)

Static power in 32nm = 68.646µm (write operation)

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 32nm = 104.49µw (read operation)

Dynamic power in 32nm = 95.175µw (write operation)

B. At 22nm

Stage 1: width = 2µm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 22nm =

Width*Length of PMOS+ Width*Length of NMOS

= 2µm*2*0.022µm+1µm*4*0.022µm

= 176nm^2

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 22nm= 1011ps

Static Power and Dynamic Power can be calculated as:

Static power in 22nm = 79.500µm (read operation)

Static power in 22nm = 108µm (write operation)

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 22nm = 208µw (read operation)

Dynamic power in 22nm = 187.92µw (write operation)

Stage 2: width = 1.5µm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 22nm =

Width*Length of PMOS+ Width*Length of NMOS

= 1.5µm*2*0.022µm+0.75µm*4*0.022µm

= 132nm^2

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 22nm= 1018ps

Static Power and Dynamic Power can be calculated as:

Static power in 22nm = 84.705µm (read operation)

Static power in 22nm = 68.646µm (write operation)

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 22nm = 217.485µw (read operation)

Dynamic power in 22nm = 95.175µw (write operation)

Stage 3: width = 1µm

The typical bit cell area is shown in the above figures as (width*length), which determines the entire area of the cell and is computed as follows:

Area of Bit Cell in 22nm =

Width*Length of PMOS+ Width*Length of NMOS

= 1µm*2*0.022µm+0.5µm*4*0.022µm

= 88nm^2

Delay can be calculated as:

Delay = (Rising Time +Falling time)/2

Delay in 22nm= 1032ps

Static and Dynamic Power can be calculated as:

Static power in 22nm = 39.935µm (read operation)

Static power in 22nm = 68.646µm (write operation)

Dynamic power = 1/2 vdd^2*Id (max)

Dynamic power in 22nm = 92.745µw (read operation)

Dynamic power in 22nm = 95.175µw (write operation)

11. Research and Outcomes of the Proposed Method

A. At 32nm

Table 2. Proposed Method Values of Power, Area and Delay in 32 nm

Type of SRAM	Variable width of Nmos µm	Width of Pmos µm	Variab le length of gate	Read		Write		Total delay ps	Area nm2
				Operation µW					
				Ps	Pd	Ps	Pd		
6T	1	2	32nm	53.2	208	137	193.5	1011	256
6T	0.75	1.5	32nm	84.3	217	68.6	95.17	1018	192
6T	0.5	1	32nm	41.3	104.5	68.6	95.17	1517	128

Table 2 contains the data collected from the simulation of a 6T SRAM cell by using 32nm CMOS technology. In the above table, the width of thePMOS and NMOS are changed and length of the gate is constant and the above values of READ and WRITE operations are obtained. The total delay and area are also obtained.

B. At 22nm

Table 3 contains the data collected from the simulation of a 6T SRAM cell by using 32nm CMOS technology. In the below table, the width of thePMOS and NMOS are changed and length of the gate is constant and the below values of READ and WRITE operations are obtained. The total delay and area are also obtained.

Table 3. Proposed Method Values of Power, Area and Delay in 22nm

Type of SRAM	Variable width of Nmos µm	Width of Pmos µm	Variab le length of gate	Read		Write		Total delay ps	Area nm2
				Operation µW					
				Ps	Pd	Ps	Pd		
6T	1	2	22nm	79.5	208	108	187.9	1011	176
6T	0.75	1.5	22nm	84.7	217.4	68.6	95.1	1018	132
6T	0.5	1	22nm	39.9	92.7	68.6	95.1	1030	88

The performance evaluation of all designs was carried out. Hence, Area and power dissipation were calculated using 35nm and 22nm by using DSCH and Microwind tools. The

performance analysis of these is observed and implemented. The results are quietly different. It was observed that, as technology size is decreased, the size of the memory also changed. So, these are the reasons the difference has been studied in this analysis.

12. Conclusion

In the existing method, 180nm, 90nm, and 45nm CMOS technologies are used to implement the 6T SRAM. The power dissipation and delay are observed in the existing method. The power is increasing gradually in the existing method, so to overcome this drawback 32nm and 22nm CMOS technologies have been used in the proposed method, where the power is found to decrease.

13. Future Scope

Further, 14nm and 7nm CMOS technologies may be used to implement the 6T SRAM and the power and delay in the 6T SRAM cell may be observed. FINFET'S and CNT FET's can also be XIV.

References

[1] Rabaey, J. M. and Pedram, M. 1996 Eds., Low Power Design Methodologies. Norwell, MA: Kluwer.

[2] K. Zhang et al., "A SRAM Design on 65nm CMOS Technology with Integrated Leakage Reduction," Symp.VLSI Circuits, pp. 294-295, June, 2004.

[3] S. Jim Hawkinson, Analysis and Performance comparison of CMOS and FinFET for VLSI applications, Muthayammal Engineering College, Rasipuram, Tamil Nādu, India, 2013. Analysis, University Teknologi Malaysia (UTM), 81310 Skudai, Johor, Malaysia, 2014.

[4] Ijjada S.R., Kumar S.V.S, Reddy M.D., Rahaman S.A., and Rao V.M. 2011 Design of low power and high-speed inverter, International Journal of Distributed and Parallel Systems (IJDPS), 2(5), pp.127- 135.

[5] K. Kanda et al., "Two Orders of Magnitude Leakage Power Reduction of Low Voltage SRAMs by Row-by-Row Dynamic Vdd Control (RRDV) Scheme ", EEE Int. ASIC/SOC Conf., Sept. 2002, vol, no., pp: 381-385.

[6] 14nm and Tam CMOS technologies to implement the 6T SRAM and observe the power and delay in the 6T SRAM cell. FINFET'S and CNT FET's can also be used in future for the implementation of the 6T SR.

[7] Lourts Deepak, Likhitha Dhulipalla, Performance Comparison of CMOS and FinFET based SRAM for 22nm technology, M S Ramaiah School of Advanced Studies, Bangalore, India, 2013.

[8] K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging." IEDM Technical Digest, 2007, pp. 247–250.

[9] Jigyasa Panchal, Dr. Vishal Ramola, Design and Implementation of 6T SRAM using FinFET with LOW POWER application, Uttarakhand Technical University, Dehradun, India, 2017.

[10] Wei Lim, Cheng Siong Lim, Michael Loong Peng Tan, Huei Chaeng Chin, Performance Evolution of 14nm FinFET Based 6T SRAM cell functionality for DC and Transient circuit.

[11] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang,B. Zheng, M. Bohr A 3-GHz 70Mb SRAM in 65nm CMOS ISSCC 2005 /SESSION 26 / NON- VOLATILE MEMORY / 26.1 Intel, Hillsboro.

[12] M. Yamaoka, et al., "0.4V Logic-Library-Friendly SRAM Array Using Rectangular-Diffusion Cell and Delta-Boosted-Array Voltage Scheme, "IEEE J. Solid-State Circuits, Vol. 39, No. 6, pp. 934-940, June, used in the future for the implementation of the 6T SRAM cell.