

# Gate Electrode Work Function Engineered Nanowire FET with High Performance and Improved Process Sensitivity

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#### **Abstract**

MOSFETs have been used in integrated circuits for a long time. These were replaced by FinFET's in 2011. But for short-channel devices, FinFET's have low performance due to various effects like velocity saturation, hot carrier effect, drain-induced barrier lowering, channel length modulation, fringing field effect, sub-threshold conduction, threshold voltage roll-off, etc. Gate All Around FET (GAA FET) is the best device that will replace the FinFET's. Therefore, during the fabrication process, it is crucial to investigate the effects of process variations caused by changes in device dimensions. This research discusses the performance of the proposed device due to process variations. The effect of changes in radius, gate oxide thickness, gate length, and channel doping on GAA FET has been discussed in detail.

**Keywords:** FinFET, Gate All Around, Process Variation, Scaling, Drive Current

## 1. Introduction

There are many design challenges for ultra scale devices. The biggest challenge is the short channel effects (SCE) [1-6]. FinFET's have replaced the conventional MOSFET's for the last few years, but their performance is compromised for highly scaled devices [7-9]. Gate All Around FET (GAA FET) will replace FinFET in the near future, as they have excellent DC

and AC characteristics as well as superior short channel performance [10-13]. Unlike FinFET, where the gate covers the channel from only three sides, GAA FETs have gates on all four sides [14-18]. So, GAA FET has better gate control which results in high drive current, high ION/IOFF, and improved sub threshold performance [19-24]. So, it is necessary to study the effects of process variation on GAA FET. Fabrication process of multi gate transistors like FinFET and GAA FET is very complex. For example, it is difficult to control the height, width and angle of inclination of the fin precisely. Similarly, it is difficult to maintain uniformity while etching the gate oxide. Surface roughness of oxide and channel interface is another issue as it can cause scattering [25].

Random placement of dopant is another serious issue which can degrade the electrical characteristics of the device. For small gate length, numbers of dopants are very less in numbers which are not easy to control during the fabrication. Variation of dopant concentration over different area of the channel degrades the device performance. The concentration of dopant can be very high near the edges and low around the centre. This is because dopant atoms have discrete nature and for very small gate length values, the average dopant concentration can vary. So, it is necessary to study the effects of process variations for better device performance and high yield and efficiency.

This paper consists of following sections – Proposed device is shown in section 2. Changes in the radius, oxide thickness, gate length and channel doping of GAA FET are discussed in section 3,4,5,6, respectively. Variation in current and threshold voltage has been shown for each variation. Finally, percentage variation in drive current and threshold voltage has been discussed in section 7. Conclusion is given in section 8.

# 2. Proposed Device

The Fig. 1. 3-D provides the schematic and 2D view of TMDG CGAA is shown in Fig. 2. In contrast to Triple Material Single Gate (TMSG) CGAA, which has an outer gate around the channel and no inner gate. This improves the ION of the device and helps to achieve high transconductance and better device performance. This is because; both the inner coaxial gate and outer gate are doing the channel inversion which results in increased number of charge carriers. Device parameters are shown in Table 1

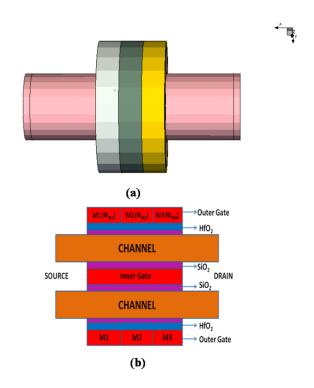
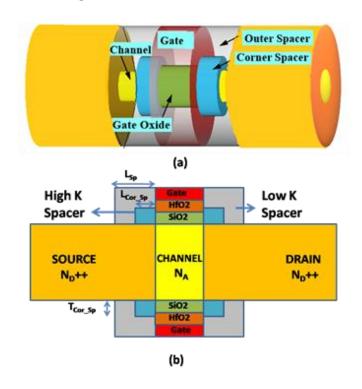


Figure 1. Structure of TMDG CGAA



**Figure 2.** (a) 3Dimensional view of TMDG CGAA, (b) 2Dimensional view of TMDG CGAA

**Table 1.** Device Parameters

| Symbol                   | Parameter                  | Value |
|--------------------------|----------------------------|-------|
| Lg (nm)                  | Length of Gate             | 10    |
| L <sub>S/D</sub> (nm)    | Length of Source/Drain     | 10    |
| R (nm)                   | Gate Radius                | 5     |
| EOT (nm)                 | Effective Oxide Thickness  | 1     |
| L <sub>Sp</sub> (nm)     | Spacer Length              | 5     |
| L <sub>Cor_Sp</sub> (nm) | Corner/Inner Spacer Length | 2.5   |

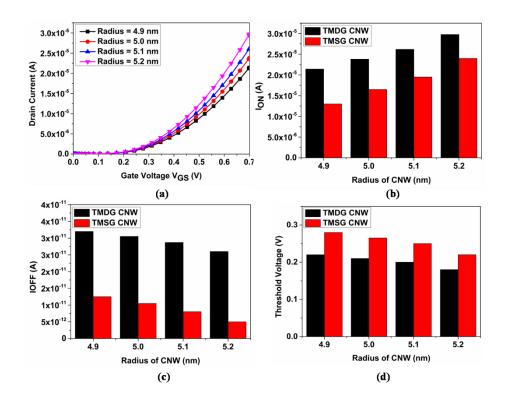
#### 3. Variation in Radius of Gate All Around FET

## 3.1 Variation of Current with Gate All Around FET Radius

ION and leakage current values are strongly dependent on device physical dimensions like radius, gate length, oxide thickness etc. Radius is the most sensitive parameter which effects device current most even due to a small variation. Variation in ION is shown in Fig. 3(a) and Fig. 3(b) whereas variation in OFF current is shown in Fig. 3(c). Variation in ION for TMDG CGAA is found to be 1.6% which is less than variation in ION for TMSG CGAA device. So, TMDG CGAA device structure should be preferred over TMSG CGAA device.

# 3.2 Variation of Threshold Voltage with Gate All Around FET Radius

The impact of variation in radius of GAA FET on threshold voltage has been studied in this work. As seen from Fig. 3(d), there is less variation in threshold voltage as radius is varied. Threshold voltage variation for TMDG CGAA is found to be 3.7%. This is one of the reason for transitioning of FinFET to GAA FET technology. As expected, the variation in threshold voltage for TMDG CGAA device structure is less than as compared to variation in TMSG CGAA device structure.



**Figure 3.** (a) Transfer Characteristics, (b) Drive Current, (c) Leakage Current, (d)

Threshold Voltage

## 4. Variation in Oxide Thickness of Gate All Around FET

## 4.1 Variation of current with Oxide Thickness

Oxide thickness effects both ION and IOFF of the device. Fig. 4(a) reveals that drive current is decreasing as oxide thickness is increasing. However, the variation in TMDG CGAA device structure is less than as compared to variation in TMSG CGAA device structure. This is because of the better gate control of TMDG CGAA device structure. Variation in drain current for TMDG CGAA device is found to be 0.54%.

# 4.2 Variation of Threshold Voltage with Oxide Thickness

Fig. 4(b) shows that the threshold voltage is increased on increasing the oxide thickness. Variation in threshold voltage for TMDG CGAA is found to be 4.8%. The variation in threshold voltage for TMDG CGAA device structure is less than as compared to variation in TMSG CGAA device structure.

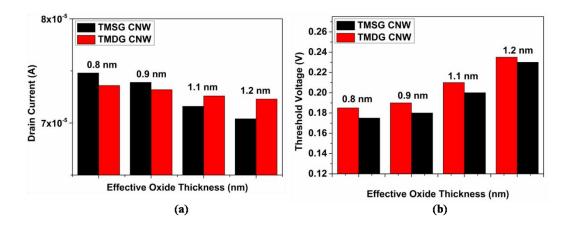


Figure 4. (a) Drain Current and (b) Threshold Voltage Versus Effective Oxide Thickness

# 5. Variation in gate length of Gate All Around FET

# 5.1 Variation of Current with Gate Length

Precise control of gate length during the fabrication process is very essential. The impact of gate length on drive current of Gate All Around FET has been shown in Fig. 5(a). Variation in  $I_{ON}$  for TMDG CGAA is found to be very less – 0.4%. This variation is very less due to superior gate control. Similarly, the variation in  $I_{OFF}$  was found to be much less. The variation in current for TMDG CGAA device structure is less than as compared to variation in TMSG CGAA device structure because of better gate control in TMDG CGAA device.

# 5.2 Variation of Threshold Voltage with Gate Length

The impact of gate length variation on threshold voltage has been analyzed in this work. Threshold voltage roll off is a SCE which can be seen in the simulation results. As seen from Fig. 5(b), there is less variation in threshold voltage ass gate length is varied. Threshold voltage variation for TMDG CGAA is found to be 4%. This is one of the reasons for transitioning of FinFET to Gate All Around FET technology. As expected, the variation in threshold voltage for TMDG CGAA device structure is less than as compared to variation in TMSG CGAA device structure.

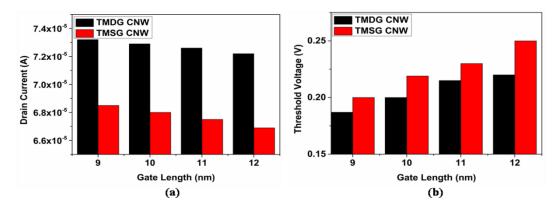


Figure 5. (a) Drain Current and (b) Threshold Voltage Versus Gate Length

# 6. Variation in Channel Doping of Gate All Around FET

# 6.1 Variation of Current with Channel Doping

Channel doping has impact on both I<sub>ON</sub> and leakage current of the device. It should be maintained precisely to achieve desired electrical characteristics of device. Fig. 6(a) shows that the drain current is decreasing as channel doping concentration is increasing. However, the variation in TMDG CGAA device structure is less than as compared to variation in TMSG CGAA device structure. This is because of the better gate control of TMDG CGAA device structure. Variation in drain current for TMDG CGAA device is found to be 2.81%.

# 6.2 Variation of Threshold Voltage with Channel Doping

Fig. 6(b) shows the changes in threshold voltage due to change in channel doping. Variation in threshold voltage for TMDG CGAA is found to be 9.5%. This change for TMDG CGAA device structure is less than as compared to change in TMSG CGAA device structure.

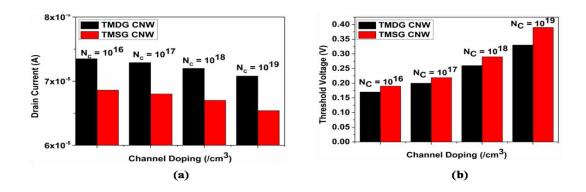


Figure .6 (a) Drain Current and (b) Threshold Voltage Versus Channel Doping

# 7. Percentage variations

Table 2 shows percentage variation in device parameters. Sensitivity of proposed device is somewhat higher to variations in radius of GAA FET. However, the sensitivity is much less to variations in other parameters like gate length, oxide thickness and channel doping.

Table 2. Percentage Variation

| Parameter   | %Variation per nm |  |
|---|-------------------|--|
| Variation in I <sub>ON</sub> with oxide thickness | 0.54%             |  |
| Variation in V <sub>th</sub> with oxide thickness | 4.8%              |  |
| Variation in I <sub>ON</sub> with gate Length     | 0.4%              |  |
| Variation in V <sub>th</sub> with gate Length     | 4%                |  |
| Variation in I <sub>ON</sub> with channel doping  | 2.81%             |  |
| Variation in V <sub>th</sub> with channel doping  | 9.5%              |  |
| Variation in I <sub>ON</sub> with radius          | 1.6%              |  |
| Variation in V <sub>th</sub> with radius          | 3.7%              |  |

Changes in drain current due to change in the radius of GAA FET is found to be 1.6% whereas threshold voltage variation due to change in radius of GAA FET is 3.7%. So, radius of GAA FET must be precisely controlled during fabrication of Gate All Around FET in order to avoid unnecessary deviation from desired characteristics. ION variation due to change in the gate length of GAA FET is found to be 0.4% whereas threshold voltage variation due to change in radius of GAA FET is 4%. Gate length sensitivity is much less than as compared to sensitivity to radius of GAA FET. Oxide thickness variation sensitivity analysis has also been done. Change in ION due to change in oxide thickness of GAA FET is found to be 0.54% whereas threshold voltage variation is 4.8%.

Finally, sensitivity due to change in channel doping was examined. It was found that variation in ION is 2.81% and variation in threshold voltage is 9.5%. In all cases, sensitivity of TMDG CGAA was found to be better than sensitivity of TMSG CGAA. This is because of the better gate control in TMDG CGAA.

## 8. Conclusion

Fabrication process of multi gate transistors like FinFET and GAA FET is very complex. For example, it is difficult to control the height, width and angle of inclination of the FinFET precisely. Similarly, it is difficult to maintain uniformity while etching the gate oxide. Surface roughness of oxide and channel interface is another issue as it can cause scattering. So, it is necessary to analyze the effects of process variation on GAA FET. The variation in device parameters due to change in dimensions, channel doping, nanowire radius and oxide thickness is within acceptable limits. So, the proposed device structure is suitable for applications which require high immunity to process variations.

## References

- [1] Kumar A, Saini S, Gupta A, Gupta N, Tripathi MM. "Chaujar R Sub-10 nm high-k dielectric SOI-FinFET for High Performance low power applications". International Conference on Signal Processing and Communication (2020): 310–314
- [2] Sreenivasulu B, Narendar V. "Performance improvement of spacer engineered n-type SOI FinFET at 3- nm gate length". International Journal of Electronic Communication 137 (2021):153803
- [3] Munjal S, Prakash NR, Kaur J. "Evolution of junctionless field effect transistors in semiconductor industry: a review". International Journal of Innov Sci Eng Technol 8(2021):94–103
- [4] Narula M S, Pandey A. "Dual-Gate Silicon Nanowire FET with a Corner Spacer for High Performance & High Frequency Applications". Journal of Electronic Materials 52, 10, (2023): 6708-6718
- [5] Das UK, Bhattacharyya TK. "Opportunities in device scaling for 3-nm node and beyond: FinFET versus GAA-FET versus UFET". IEEE Tran Electron Devices 67,6, (2020):2633–2638

- [6] Mohan C, Choudhary S, Prasad B. "Gate all around FET: an alternative of FinFET for future technology nodes". International Journal of Advanced Research Science Engineering 6,7, (2017):561–569
- [7] Nagy D, Indalecio G, Garcia Loureiro NJ. "FinFET versus gate-all-around nanowire FET: performance, scaling, and variability". J Electron Devices Soc 6 (2018):332–340
- [8] Narula M S, Pandey A. "Performance Evaluation of Stacked Gate Oxide/High K Spacers Based Gate All Around Device Architectures at 10 nm Technology Node". Silicon 14,5 (2022): 2397 – 2407
- [9] Kumar S., Goel E. "2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs With a SiO<sub>2</sub>/HfO<sub>2</sub> Stacked Gate-Oxide Structure". IEEE Transactions on Electron Devices 64,3 (2017): 960-968
- [10] Y. Li, H.-M. Chen, S.-M. Yu, J.-R. Hwang, and F.-L. Yang. "Strained CMOS Devices with Shallow-Trench-Isolation Stress Buffer Layers". IEEE Transactions on Electron Devices 55,4 (2008):1085-1089.
- [11] Hui-Wen Cheng, C. -H. Hwang and Y. Li. "Propagation delay dependence on channel fins and geometry aspect ratio of 16-nm multi-gate MOSFET inverter". 1st Asia Symposium on Quality Electronic Design (2009):122-125
- [12] Vallabhuni RR, Yamini G, Vinitha T. "Performance analysis:D-Latch modules designed using 18nm FinFET Technology". International Conference on Smart Electronics and Communication September (2020): 1169–1174
- [13] Kajal, Sharma VK. "Design and Simulation of FinFET Circuits at Different Technologies". International Conference on Inventive Computational Technologies (2021): 1–6
- [14] Narula M S, Pandey A. "Gate Engineered Silicon Nanowire FET with Coaxial Inner Gate for Enhanced Performance". Silicon 15 (2023): 4217 4227
- [15] Zhang S. "Review of Modern Field Effect Transistor Technologies for Scaling". 2nd International Conference on Electronic Engineering and Informatics 16 (2020)
- [16] Uddin M, Athiya M, Masud NLA, Chowdhury H. "FinFET based SRAMs in sub-10nm domain". Microelectronics Journal 114,5 (2021):105116
- [17] Ratnaa VR, Sarithab M, Saipreethi V, Vijayb PC, Shaker MD, Sadullae S. "High speed energy efficient multiplier using 20nm FinFET technology". International Conference on IoT based Control Network Intelligent Systems (2020)

- [18] Narula M S, Pandey A. "A Comprehensive Review on FinFET, Gate All Around, Tunnel FET: Concept, Performance and Challenges". IEEE International Conference on Signal Processing & Communication (2022): 554-559
- [19] Gadarapulla R, Sriadibhatla S. "Tunnel FET based SRAM cells a comparative review". Int Conf Microelectron Devices Circuits System 1392 (2021):217–228
- [20] Kim SD, Guillom M. "Performance tradeoffs in FinFET and gate all around device architectures for 7 nm node and beyond". IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (2015): 1–3
- [21] Mohan C. "Gate all around FET: an alternative of FinFET for future technology nodes". Int J Adv Res Sci Technol 6(2017):561–569
- [22] Liu TY, Pan FM. "Characteristics of gate-all-around Junctionless polysilicon nanowire transistors with twin 20-nm gates". J Electron Dev Soc 3(2015):405–409
- [23] Zhuge J, Wang R, Huang R, Tian Y, Zhang L, Kim D-W, Park D, Wang YY. "High-performance silicon nanowire gate-all-around nMOSFETs fabricated on a bulk substrate using CMOS compatible process". IEEE Electron Device Lett 31(2009):57–60
- [24] Huang R, Wang R, Zhuge J, Liu C, Yu T, Zhang L, Huang X, Zou J, Liu Y, Fan J, Wang Y. "Characterization and Analysis of Gate-All-Around Si Nanowire Transistors for Extreme Scaling". IEEE Custom Integrated Circuit's Conference (2011): 1–8
- [25] Moezi N, Karbalaei M. "Predictive physics based simulation of Nano scale gate-all-around field effect transistor under the influence of high-k gate dielectrics". J Nanostruct 10(2020):736–743