

Analysis of 10 nm Strained Channel Double Gate Ultra-Thin Body Junctionless MOSFET

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Abstract

Numerous technological improvements and innovative device architecture have been thoroughly explored and tested for continually downscaling components without compromising on performance metrics. The most simplified structure that has been introduced so far is the junctionless transistors. Junctionless transistors have been shown to exhibit excellent electrical behavior with improved short-channel effects. The major challenges with junctionless based transistors are low ON-current drive and high device variability. Strain engineering has been proven to be a viable option to enhance the ON-current performance of the MOSFET. This work incorporated strained silicon in double gate junctionless ultra-thin body MOSFET (DG-JL UTB MOSFET), which enhanced the mobility of the charge carrier as a result of which ON current behavior improves. The simulated results show 30.2% enhancement in the ON-current, subthreshold current reduced to nearly half, I_{ON}/I_{OFF} ratio is increased by three times, and Drain-induced barrier lowering (DIBL) reduced by 25.1% with respect to unstrained device. Analog performance metrics are also calculated for the considered device design. With strained silicon, the value of G_m is increased by more than 30% and transconductance generation factor (TGF) is increased by 28.27% in reference with the unstrained device.

Keywords: Junctionless Transistor, Ultra-Thin Body MOSFET, Strained Silicon, Strain Engineering

1. Introduction

Junctionless based FETs (JL FETs) have emerged as a simplest device structure that solves the critical problem of forming highly quality p-n junction in deep nanoscale domain. Unlike conventional inversion-mode devices, JL FETs uses same doping type (either n-type or p-type) in all the three regions: source, drain, and channel region [1]. In order to ensure the high drive current, JL FETs require high doping concentration ($\sim 10^{18} \text{ cm}^{-3}$ - 10^{19} cm^{-3}) in all the three regions, that poses many serious challenges [2]. The main issues are high device-to-device variations and low current drive that need to be taken care of.

Though silicon remains as a best material for MOSFET in present scenario, maintaining device performance with downscaling remains challenging. To sustain the inevitable trend of device miniaturization without compromising with the performance, numerous technological improvements, such as channel engineering, III-V channel material, gate engineering, and spacer engineering have been explored and studied by many research groups [3-7]. In this direction, incorporation of strained silicon in the channel region has been rigorously studied and investigated. The strained silicon has been proven viable option to enhance the carrier mobility and thereby improve the ON current of the device [8-9]. Compared to the conventional MOSFET where different type of doping is used in source, channel, and drain regions, incorporation of strained silicon in Junctionless device is expected to be less challenging due to its homogenous doping.

This work investigated the impact of strain engineering on Double Gate Junctionless Ultra-Thin Body MOSFET (DG-JL UTB MOSFET) for 10nm channel length. The strained Si channel is a key feature of the design. In this work, the strained Si film without the presence of SiGe layer has been used to minimize the issues such as poor thermal conductivity, high leakage current, Ge diffusion into strained Si, and misfit dislocations. The considered structure combines the benefit of UTB, JL architecture and strain engineering, therefore expected to shows superior short channel and ON-state behaviour. The detailed design structure and simulation methodology is presented in Section 2. Section 3 contains a detailed comparative analysis of Strained DG-JL UTB MOSFET with its unstrained counterparts. The research is concluded in the last section.

2. Device Structure and Simulation Framework

For statistical device simulation, Sentaurus TCAD platform is used. A proper device calibration has also been carried out beforehand to ensure the authenticity of the obtained results. Figure 1 shows the two-dimensional view of DG-JL UTB MOSFETs simulated in this research. For gate dielectric, silicon dioxide (SiO_2) is used, while for spacer material, Hafnium oxide (HfO_2) is used. To design strained DG-JL UTB MOSFETs, the strained silicon -on-insulator (SSOI) technique is used [10]. With strained silicon, a biaxial tension is induced in the thin body film and its band structure changes. This consequently reduces the effective mass of carriers and thereby increases their mobility. So, the drive current performance is expected to increase by employing strained channel. All other physical design parameter is chosen as per International Technology Roadmap for Semiconductors (ITRS) projection for gate length 10 nm which are tabulated in Table 1 [11].

The electrical behavior of DG-JL UTB MOSFETs with and without strained silicon has been analyzed by including following mathematical models in the physics section [12]:

1. Mobility models including doping dependence and electric field dependence.
2. Lombardi Mobility model for including effect of surface mobility degradation.
3. Bandgap Narrowing (BGN) model to account the impact of high doping concentration.
4. Shockley–Read–Hall (SRH) recombination with doping-dependent lifetime.
5. Density Gradient model to incorporate carrier quantization effects.
6. Strain Mobility model to account the impact of strain engineering.

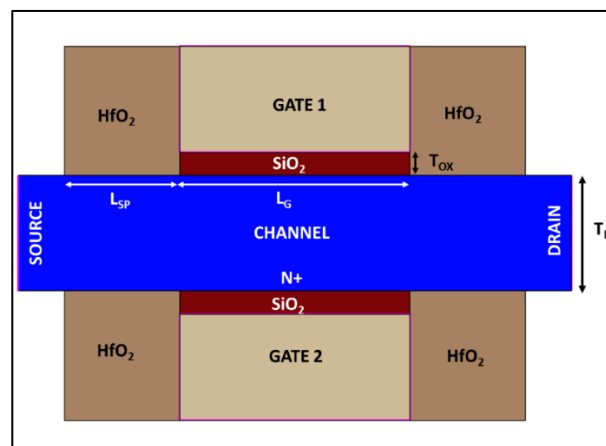


Figure 1. Device Structure of DG-JL UTB MOSFET

Table 1. Design Parameters

Parameter	Value
Channel Length (L_G)	10 nm
Body Thickness (T_B)	5 nm
Oxide Thickness	1 nm
Doping Concentration (N_D)	10^{19} cm^{-3}
Spacer Length (L_{SP})	5 nm
Gate Workfunction	5 eV
Supply voltage (V_{DD})	0.7 V

3. Results and Discussion

3.1 Electrostatic Behavior

The simulated current-voltage characteristics of strained DG-JL UTB MOSFET and unstrained DG-JL UTB MOSFET is shown in Figure 2. From the figure, it can be clearly seen that the incorporation of strained silicon film in the device under consideration not only improves the current drive but also exhibited better OFF condition behavior. This consequently results in better switching behavior of strained engineering device. The high ON-state current of strained devices is due to high carrier mobility in tensile stretched silicon layer. The various performance metrics extracted from these curves are summarized in Table 2. The value of threshold voltage is measured using a constant current method (at $V_{DS}=0.7V$). The strained devices outperform its unstrained counterpart in terms of short channel behavior. For strained DG-JL UTB MOSFET, the ON-current increased by 30.2%, subthreshold current is reduced by 58.8%, I_{ON}/I_{OFF} ratio is increased by three times, and DIBL reduced by 25.1% with respect to unstrained device. Also, subthreshold slope shows almost negligible change. Hence, inclusion of strain engineering can be considered as a suitable option for low power applications.

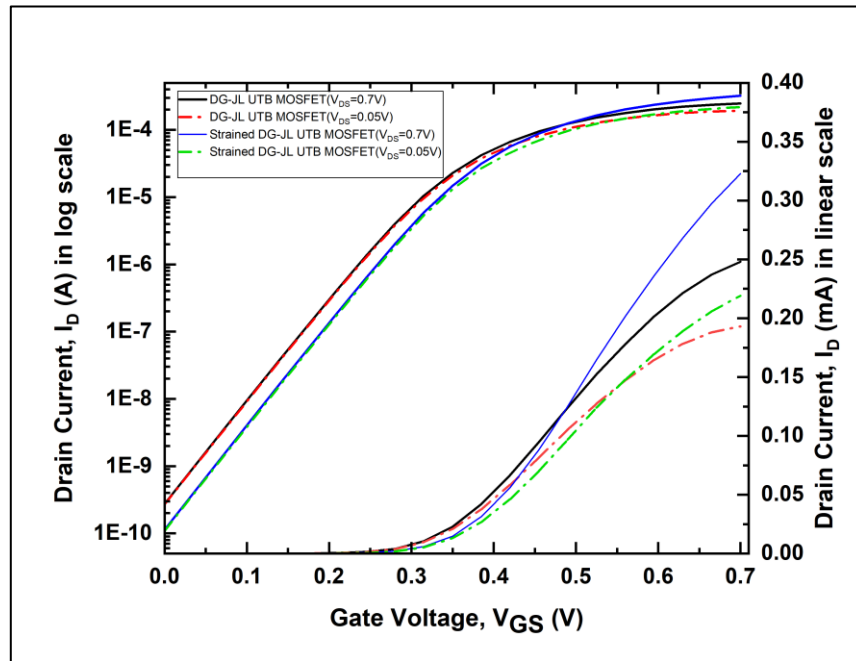


Figure 2. ID-VGS Curve for DG-JL UTB MOSFET With and Without Strained Silicon

Table 2. Comparison of Strained DG-JL UTB MOSFET and DG-JL UTB MOSFET

Parameter	Strained DG-JL UTB MOSFET	DG-JL UTB MOSFET
Threshold Voltage (V_T)	0.351 V	0.331 V
On-Current (I_{ON})	3.2281e-04 A/um	2.4787e-04 A/um
Subthreshold Current (I_{Sub})	1.1483e-10 A/um	2.7864e-10 A/um
I_{ON}/I_{OFF}	2.8113e+06	8.8955e+05
Subthreshold Slope (SS)	73.488 mV/dec	73.594 mV/dec
DIBL	223.4895 mV	298.4922 mV

3.2 Analog Performance

Figure 3 shows the impact of strained silicon on the transconductance (G_m) and transconductance generation factor ($TGF=G_m/I_D$) in DG-JL UTB MOSFET. With strained silicon, the value of G_m is increased by more than 30% in reference with the unstrained device. Higher G_m indicates better analog performance in terms of gate control over the channel.

Another metric TGF indicates the effectiveness of FET to convert DC current into an AC frequency. The improvement of 28.27% in TGF is observed with strained engineering device.

Figure 4 shows the variation of output transconductance (G_D) with gate voltage (V_{GS}) for unstrained and strained DG-JL UTB MOSFET. Almost same G_D is observed for both the devices. The obtained results indicated that strain engineering can contribute to an overall significant improvement in analog performance of device.

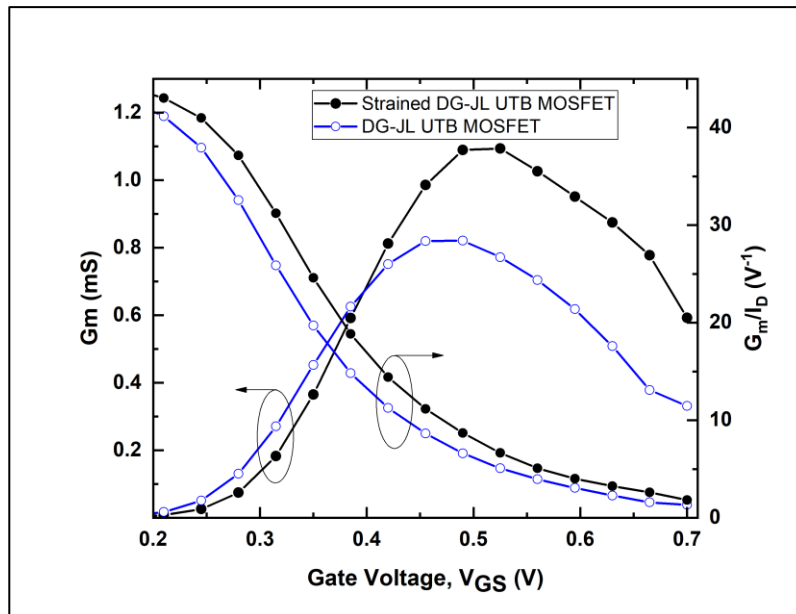


Figure 3. Variation of G_m and G_m/I_D with Gate Voltage for DG-JL UTB MOSFET With and Without Strained Engineering at $V_{DS}=0.7V$

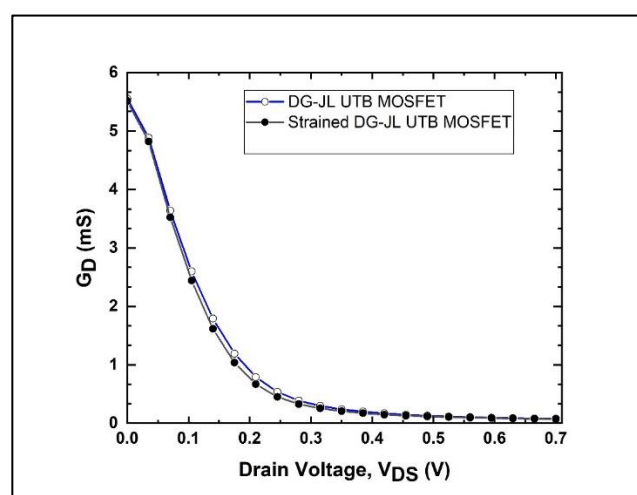


Figure 4. Variation of G_D and VEA with Drain Voltage for DG-JL UTB MOSFET With and Without Strained Engineering at $V_{GS}=0.7V$

4. Conclusion

The study reported the effect of strain engineering on a 10 nm DG-JL UTB MOSFET structure. Simulated results show that replacing silicon with strained silicon layer in the device structure leads to significant improvement in short channel effects. Furthermore, the device under study presented better analog performance compared to its unstrained counterparts. Hence, as a future perspective, the strain silicon can be used as a good alternative material for low power and faster switching application devices. However, from the fabrication point of view, further investigation is required for its feasibility at such a nanoscale domain.

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Author's biography

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