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Design and Implementation of High Speed 6 – bit Current Steering DAC Modelling using Cadence

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Abstract

The research presents a streamlined approach for modelling Current Steering Digital-to-Analog Converters (DACs) by using ideal current sources. DACs are essential components in electronics, converting digital signals into analog voltages or currents. Traditional modelling methods can be intricate and computationally demanding. The proposed method abstracts DAC behaviour using ideal current sources, specifically customized for 6-bit Current Steering DACs. This simplified model offers practical benefits for system-level simulations and rapid prototyping, featuring reduced complexity and enhanced speed. Additionally, the research explores increasing the sampling rate from 300MHz to 500MHz, opening up potential applications in fields such as audio processing and industrial automation. This approach presents a promising direction for DAC design and optimization, addressing the evolving needs of modern electronic systems.

Keywords: DAC, Current Steering, Electronic Systems, Audio Processing, Industrial Automation.

1. Introduction

A 6-bit current steering Digital-to-Analog Converter (DAC) translates digital signals into precise analog currents, that play an essential role in high-speed and high-fidelity

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applications such as communication systems, video processing, and instrumentation [1-3]. This type of DAC uses a network of binary-weighted current sources and switches to steer the appropriate amount of current to the output, corresponding to the digital input code [4-7].

Key design considerations for a 6-bit current steering DAC include accuracy, linearity, and speed. Ensuring minimal differential nonlinearity (DNL) and integral nonlinearity (INL) is critical for high precision. The DAC must also switch currents rapidly to handle high-speed digital inputs without significant delay or distortion. The basic block diagram of 6-bit Current Steering DAC (CS -DAC) is shown in Figure 1 [8-10].

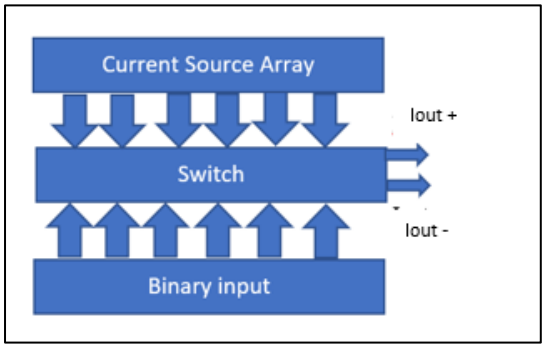

Figure 1. Block Diagram Of DAC.

2. Proposed Methodology

The proposed methodology for the modeling of current steering DAC consists of a few blocks which include an Ideal current source, switches, top-level design of those current source blocks which is binary weighted, and an additional non-overlapping clock generator is deployed to minimize the glitches in the output. Figure 2 illustrates the schematic of the proposed DAC.

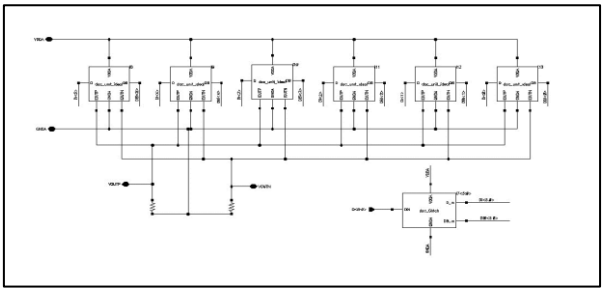

Figure 2. Proposed DAC Schematic

A. Ideal Unit Current Source

Ideal Current Source: This research uses a novel approach to implement the ideal current source by adding a very high external resistance parallel to the current source. This approach aids in obtaining an ideal current source that passes the current through the same terminal due to its low resistance compared to the other terminal. Figure 3 illustrates ideal unit current source schematic.

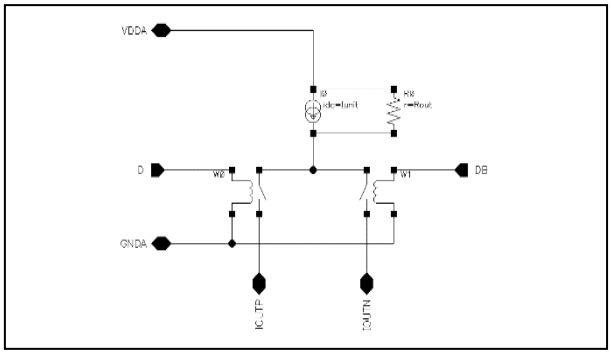

Figure 3. Ideal Unit Current Source Schematic

Switches: The main use of the switches is to regulate the current flow in the circuit. In this research, the switches block and current sources block are combined to get a better understanding and working of the circuit. The switches are deployed with minimum Ron resistance and max Resistance when in the off state.

B. Top Level DAC

Top Level DAC: Using all the primary current sources and switches blocks the top level of the DAC is built. In this stage, all the six blocks of ideal current sources are binary weighted and are mapped onto the 6 bits inputs. Figure 4 illustrates the schematic of Top level DAC.

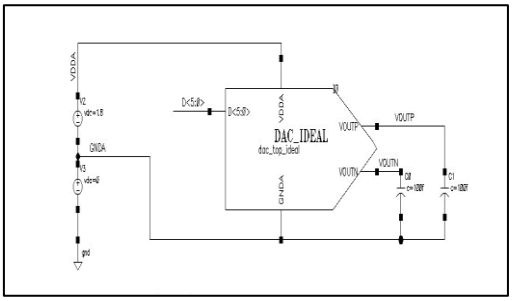

Figure 4. Top Level DAC.

C. Non-Overlapping Clock Circuit

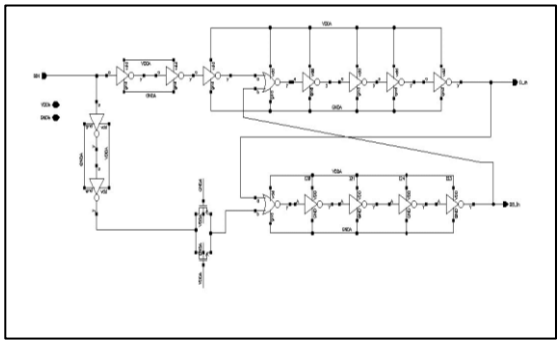

Figure 5 . Non-Overlapping Clock Circuit

Non-Over Clock Generator: The non-overlapping clock generator consists of a series of inverters which in turn decreases the glitches obtained in the absence of it and it also increases the delay of the output. Figure 5 illustrates the non-overlapping clock circuit.

3. Results and Discussion

In the proposed research ideal 6-bit CS-DAC is implemented in CADENCE 180nm process technology with an improved sampling rate from 300Mhz to 500Mhz. The test circuit is shown in Figure 6. The circuit consists of a digital input section, a DAC conversion block, and an analog output section. In the digital input section, a clock source (VCLK) generates timing signals, while a 6-bit digital input (D<5:0>) is provided to the DAC. The DAC_IDEAL block converts the digital signals into an analog output voltage, utilizing a power supply (VDD and GND). The DAC produces two differential outputs, VOUTP (positive output) and VOUTN (negative output), which are then processed through a capacitor-resistor network. This network, consisting of capacitors (C1, C2) and resistors, is likely used for signal filtering and stabilization. Finally, the processed signal is directed towards the VOUT terminal, providing the desired analog output. This circuit effectively demonstrates the digital-to-analog conversion process, which is essential in applications such as audio processing, signal generation, and data acquisition systems.

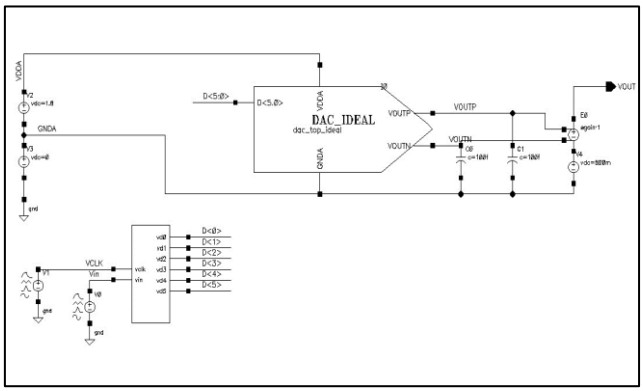

Figure 6. Test Bench for 6-bit Current Steering DAC.

In the test circuit, the ideal analog-to-digital converter (ADC) is implemented from AnalogLIB library to convert the sine wave into digital code and provide these digital data as input to a 6-bit ideal current steering DAC circuit. The 6-bit ideal ADC block is designed by editing the Verilog code of the 8-bit ideal ADC. Figure 7 illustrates the output of 6-bit Ideal ADC for ramp input.

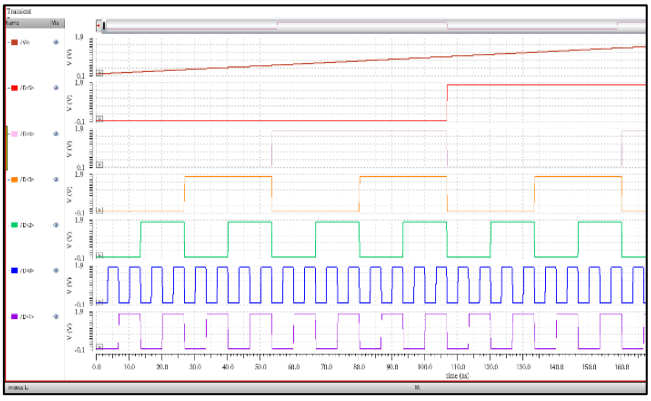

Figure 7. Output of 6-bit Ideal ADC for Ramp Input

The implemented ideal DAC is simulated for sampling rate of 300MHz and 500MHz. Figure 8 illustrates the simulation for 300MHz for Ramp input.

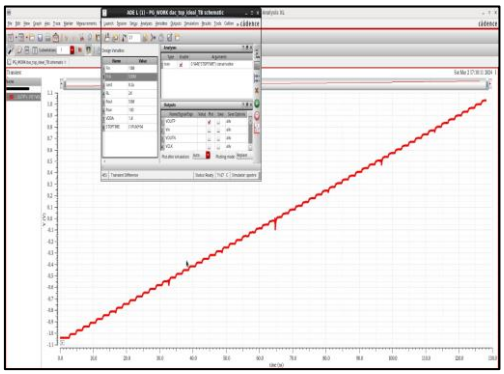

Figure 8. Simulation for 300MHz for Ramp Input

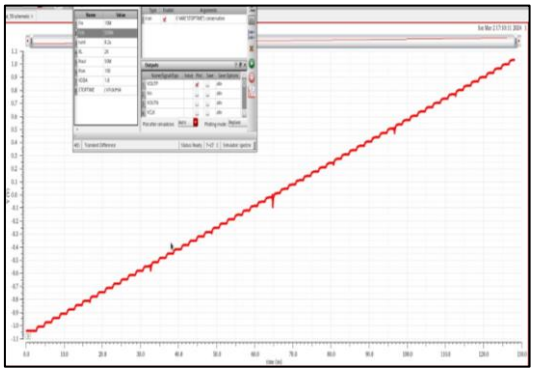

Figure 9. Simulation for 500MHz

To avoid simulation of the DAC for 300MHz or 500Mhz than the required time period. The full scale of the DAC is linked to the sampling frequency (Fclk) by assigning a variable for transient time e, VAR("STOPTIME").

$$STOPTIME = 1/Fclk \quad (1)$$

Figure 9 illustrates the simulation for 500MHz

Table 1 shows the performance parameters used for modeling the DAC to 500MHz sampling rate.

Table 1. Performance Parameter

Parameters	Value
Technology	0.18um
Resolution	6
Conversion Rate	500MHz

Supply Voltage	1.8V
Effective Voltage (Veff)	0.9V
SFDR	44dB
INL	< 0.8LSB
ENOB	5.2198bits

The static and dynamic parameters like INL (Integral Non-Linearity), DNL (Differential Non-Linearity), and spectrum analysis have been plotted for the designed Ideal 6-Bit DAC using the CADENCE ADE calculator.

Static and Dynamic Characteristics

1. Signal to Noise Ratio (SNR):

$$SNR = 6.02 * N + 1.76 \quad (2)$$

N=Number of input bits.

2. Signal-to-Noise and Distortion Ratio (SNDR):

$$SND = SNR + THD \quad (3)$$

3. Total Harmonic Distortion (THD):

$$THD = \frac{1}{SFDR} \quad (4)$$

4. Effective Number of Bits (ENOB):

$$ENOB = (SNR - 1.76)/6.02 \quad (5)$$

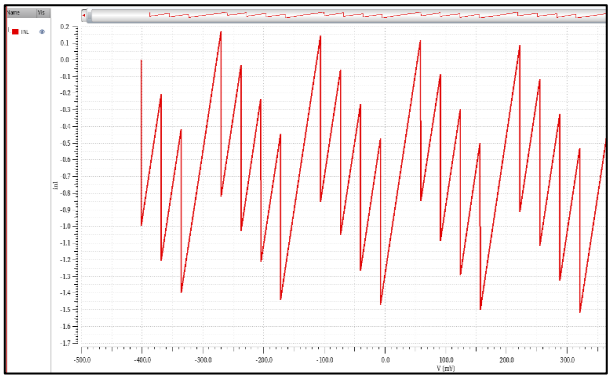

Figure 10. INL Plot

The Integral Non-Linearity (INL) plot in Figure 10 illustrates the deviation of a Digital-to-Analog Converter (DAC) from its ideal transfer function. The X-axis represents the input digital code, while the Y-axis shows the INL error in LSB (least significant bit) deviation. The

red line indicates the INL variation across different input values, revealing systematic non-linearity likely caused by a mismatch in current sources within the Current Steering DAC. The periodic nature of the plot suggests recurring errors, which can degrade the DAC's accuracy and introduce distortion in signal conversion. Additionally, the upper panel provides a smoothed representation of the INL behavior. High INL values indicate significant deviation from ideal performance, affecting precision applications such as high-speed communications and audio processing. Addressing these non-linearities is essential for improving the DAC's overall accuracy and performance.

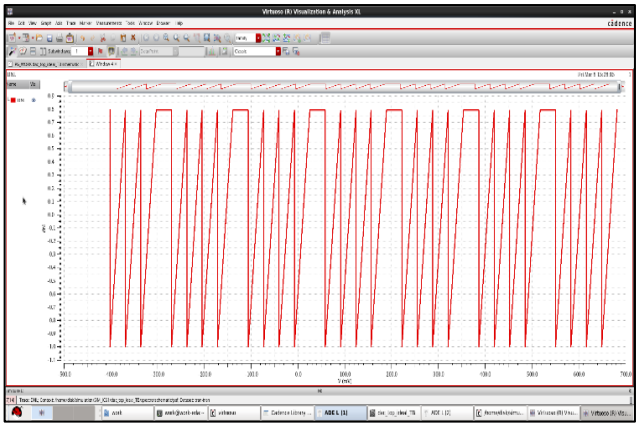

Figure 11. DNL Plot

The DNL plot in Figure 11 evaluates the deviation of step sizes between adjacent digital codes from the ideal step size, ensuring linearity and detecting potential missing codes if deviations exceed ±1 LSB.

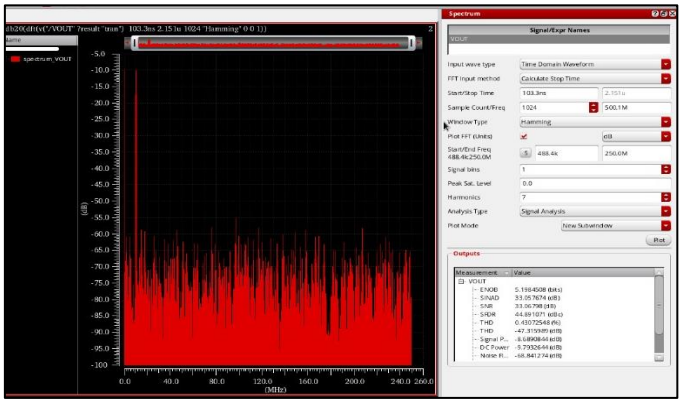

Figure 12. Spectrum Analysis using Hamming Window

Figure 12 illustrates the spectral analysis for samples of 1024 with a sampling frequency of 500MHz under the Hamming window.

This spectrum analysis helps in evaluating the signal integrity of the 6-bit DAC, ensuring that unwanted harmonics and noise components remain within acceptable limits for applications requiring high precision in digital-to-analog conversion

4. Conclusion

In this proposed research CS DAC is implemented on CADENCE TSMC 180nm process technology with an improved sampling rate from 300MHz to 500MHz.These modelled DAC specifications are used to implement the transistor level. The proposed DAC design provides SFDR of 44dB by using a Hamming window for 1024 samples. The sampling rate of 500MHz is achieved in the designed current steering DAC. Simulation of this high-speed 6-bit current steering DAC circuit is done using spectre simulator of CADENCE and improved simulation results are obtained.

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