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Machine Learning Algorithms Performance Analysis for VLSI IC Design

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Abstract

The design of an analogue IC layout is a time-consuming and manual process. Despite several studies in the sector, some geometric restrictions have resulted in disadvantages in the process of automated analogue IC layout design. As a result, analogue design has a performance lag when compared to manual design. This prevents the deployment of a large range of automated tools. With the recent technical developments, this challenge is resolved using machine learning techniques. This study investigates performance-driven placement in the VLSI IC design process, as well as analogue IC performance prediction by utilizing various machine learning approaches. Further, several amplifier designs are simulated. From the simulation results, it is evident that, when compared to the manual layout, an improved performance is obtained by using the proposed approach.

Keywords: VLSI, IC design, placement, performance analysis, machine learning

1. Introduction

The process of designing the layout of an analog integrated circuit (IC) is a manual process. When compared to the highly automated digital counterpart, there is a sharp contrast to this technology [1-2]. Various intertwined factors contribute towards this difference. A prominent Resistance and Capacitance (RC) parasitic are created in the layout, which has a significant influence on the performance of the analog circuit [3]. The Operational Transconductance Amplifier (OTA) and its post-layout simulation as well as pre-layout

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schematic performance characteristics are contrasted. The unity gain frequency, bandwidth and DC Gain characteristics comparison shows that a unity gain frequency loss of around 22% may be observed due to the layout [4]. Accurate and quick estimation of the layout effect on performance is challenging and complex. When compared to the digital circuits, the performance of analog circuits are vast. Different types of analog circuits use different performance metrics [5]. In Phase Locked Loop (PLL) circuits, evaluation of settling time, linearity in analog to digital converter (ADC) and digital to analog converter (DAC), phase margin, bandwidth and gain in operational amplifiers are some examples of the diverse circuits and parameters. Evaluation of simulation and multiple trial layout iterations are performed by experienced designers in analog IC layout. A design bottleneck is formed due to this time consuming process [6].

For several decades, extensive studies are undertaken pertaining to automated analog IC design [7]. Common centroid, symmetry and other geometrical constraints are faced during these design processes of analog ICs as seen in most of the existing literature [8]. During the presence of variations, these constraints contribute to the performance deviations hindering the achievement of the nominal and desired performance. The geometric constraints are derived from the performance constraints in analog IC layout while estimating the chip design and performance. It is challenging to find a feasible solution with unnecessarily tight geometric solutions due to simplified multiple performance characteristic interactions [9-11]. Analog IC placement influences the performance of circuit directly as observed by certain researchers. In analog circuits, generalization of several nonlinear behavior is hard due to the simple linear model used for performance estimation [12]. Several researchers have implemented special performance based constraints in the placement of analog ICs. However, in general cases, these constraints are not considered. The circuit performance can be considered with several sizing solutions for layout migration using neural network algorithms [13]. In case of wide applications, mature and well researched analog IC layout techniques are not available for achieving automated performance.

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The performance of analog ICs is enhanced by using an automated approach by implementing machine learning technique in this paper. The circuit performance encounters first order effect through placement as the distance among pins decides the wire parasitic. The circuit performance is optimized directly and it is compared to the existing constraint based techniques. In comparison with the linear models the performance models based on machine learning technology is superior due to their ability to handle nonlinear behavior [14]. Random forest, neural network, support vector machine (SVM) and various machine learning techniques are analyzed and compared. Without layout design, voluminous training data are obtained using data preparation and feature selection schemes that are developed for the prediction of circuit performance using machine learning [15]. Along with precision and accuracy, the fidelity of machine learning model is analyzed. In VLSI circuit design, the fidelity of machine learning model is analyzed by very few researchers. This paper also proposes an IC placement technique that is performance driven [16]. Along with the symmetry constraints, geometry constraints, area and wirelength, the conventional objectives, the performance of the analog circuit can be optimized directly. For multiple OTA design placements, the proposed model is implemented. In comparison with the conventional automatic placement, the proposed approach offers improved performance according to the simulation results of the post layout model [17]. In case of faster magnitude orders, the manual layout performance is attained.

2. Related Works

Since the past few decades, the automated analog IC layout is studied by several researchers. In the digital design floor planning, simulated annealing framework is followed for analog IC placement in most of the existing literature [18]. However, common centroid, symmetry and such additional geometric constraints are considered. B-tree representation or sequence pair is used for enforcing the geometric constraints in most cases [19]. In some cases, the performance of the analog circuit are not addressed directly while exploring the analytical approaches [20]. The layout geometric constraints are obtained from the performance constraint in order to notice the performance of the layout impact [21]. In order to satisfy the

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specifications of performance, there is an insufficiency or overly tight geometric constraints obtained leading to the dilemma while capturing the complex relationship between performance and layout [22]. As a result, the level of sophistication of such change is insufficient. Certain researchers [23] suggest a layout strategy that is directly performance oriented. However, such techniques are inefficient when dealing with nonlinear features since linear approximation is employed to estimate performance [24]. Monotonic current path constraints are used for addressing the performance of analog IC. However, rather than being common for various metrics, certain performance characteristics are restrict the efficiency of this technique.

For the design of analog ICs, various machine learning schemes are investigated in the recent days [25]. Without the performance consideration, in order to perform layout migration, neural network technique is used [26]. The legacy design patterns may be reused using knowledge mining scheme without any direct performance consideration [27]. Analog parameter tuning based on reinforcement learning is proposed in certain literature [28]. The RF passive templates are generated by applying graph neural network techniques [29]. Despite various studies on analog ICs and performance driven placement, the research in this domain is currently insufficient [30].

3. Methodology

Minimization of composite objective functions such as circuit performance, wirelength, area and satisfaction of symmetry and other geometric constraints is made possible with the circuit design rules where all passive devices and transistor placement locations are determined with the process technology file, schematic description or analog circuit netlist. The analog placement used widely in previous works use simulated annealing based placement algorithm. Various types of cost functions are incorporated with vast flexibility using simulated annealing technique. When compared to digital circuits, the elements in this algorithm are lesser and hence for analog IC design, an acceptable runtime speed is obtained despite not being a

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generally fast algorithm. Machine learning model is used along with the cost function for capturing the circuit performance which is a major variation from the existing work. The performance is predicted by the machine learning model when a placement solution is offered. Amplifiers and other analog circuits may be solved using the proposed approach as it aids in overcoming the huge challenge of analog placement in a performance driven manner. Several machine learning schemes are available that may be used in this work. Support vector machine (SVM), Naïve Bayes (NB), Random Forest (RF) and Artificial Neural Network (ANN) are investigated in this paper.

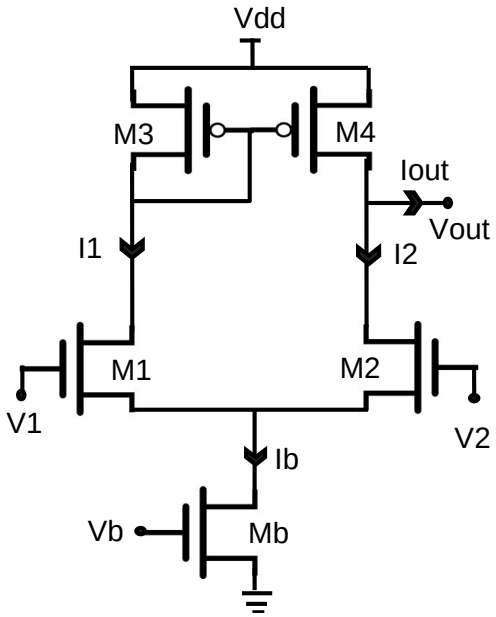

Figure 1. Operational Transconductance Amplifier – Multi-pin Net Model

Figure 1 provides the multi-pin net model of an operational transconductance amplifier (OTA). One layout solution may be used for generating several samples of training data using the star model. Parasitic extraction is performed on obtaining the complete layout with routing after obtaining the circuits' arbitrary legal placement. While retaining the transistor parasitic, a template is formed by removing the extracted netlist wire parasitics. One training sample is obtained by inserting each net of the template with a random star model. Logistic regression

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is used in the machine learning model. Simulated annealing framework is used by the placement algorithm. Sequence pairs are used for describing the circuit elements and the relative spatial order. Common centroid, symmetry and other geometric constraints may be enforced easily with this model. Simulated annealing enables considering the cost function of the system.

4. Results and Discussion

A 256G memory, 2.8 GHz frequency and Xeon (R) E5-2680 V2 processor based Linux system is used for conducting the experiments. Python language is used for creating the machine learning models. C++ programming is used for router and analog IC placer. Design and layout rule checking is performed along with extraction of netlists using SPICE simulation. For the purpose of experimentation, a 9nm process technology ASAP is used. Telescopic OTA, folded-cascode OTA and two stage OTA designs are used for evaluation of the proposed technique. For each net, the wirelength is varied randomly and generation of a thousand layout annotated schematics is performed for each design which is further simulated and the training data is obtained. 60% of the samples are used for training and 40% for testing out of the 1000 samples. The hyperparameters of the model are tuned by performing cross validation while constructing the model.

The input feature size is equal to the number of nodes in every layer of the three hidden layered neural network structure. In this experiment, each random forest has less than 500 trees with a height of less than ten metres. For SVM, the regularization parameter is set to 1, and the radial basis function kernel is used. Phase margin, bandwidth, unity gain frequency and gain of the machine learning model is estimated as represented in figure 2-5. For different OTA designs and various circuit characteristics, the model accuracy is further analyzed and estimated. The simulation results provide the optimal reference for the layout annotation. While predicting the circuit characteristics, the errors lead to inconsistency between the optimal reference and model prediction.

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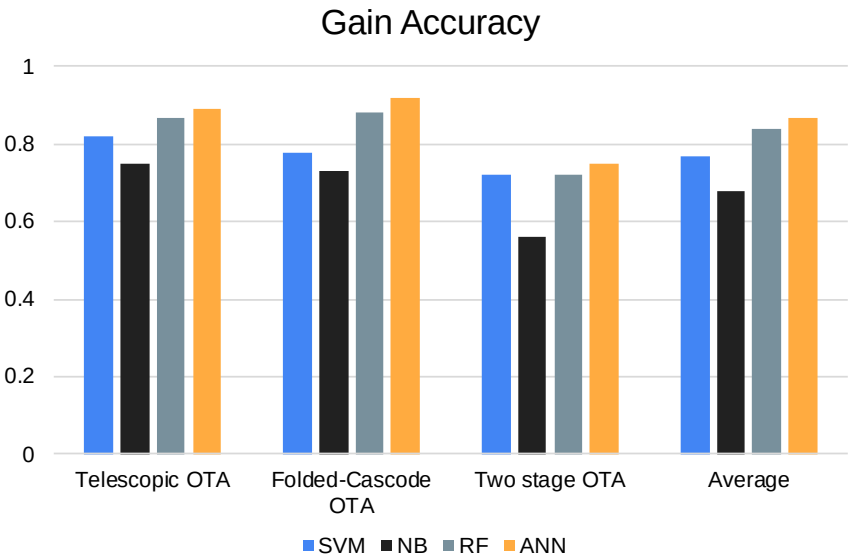

Figure 2. Machine Learning Model Gain Accuracy

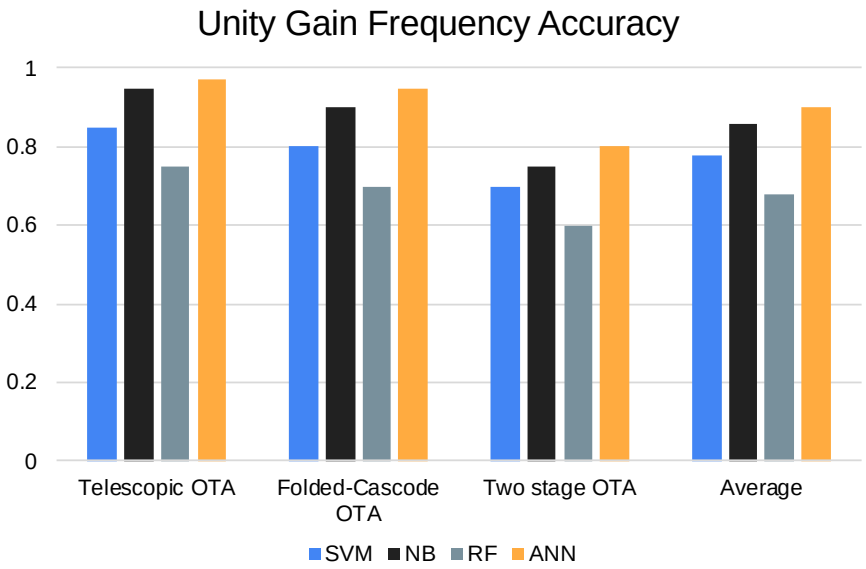

Figure 3. Machine Learning Model Unity Gain Frequency Accuracy

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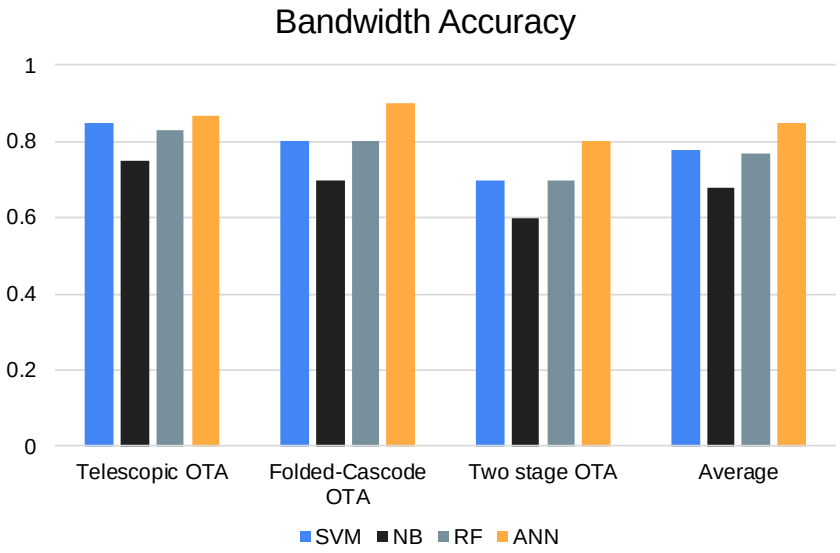

Figure 4. Machine Learning Model Bandwidth Accuracy

Further, the post-layout simulation fidelity results and the corresponding optimal reference values are obtained. When compared to the model input features of machine learning, the layouts actual wirelength may vary considerably. While predicting the circuit characteristics, besides errors, other inconsistencies may be faced due to this discrepancy. When compared to ANN and NB, SVM and RF offers improved post-layout wirelength prediction. However, the circuit performance prediction is enhanced using ANN. Conventional automatic placement and manual layout are compared and the machine learning based placement performance is estimated. Post-layout simulation offers the performance characteristics of individual circuit. The runtime cost of computation is also compared. Placement, routing and total time is estimated for all the OTA types. When compared to the manual design, the magnitude of machine learning model is faster. The layout designs also address the symmetry constraints. In folded cascaded OTA, a shorter post-layout wirelength is observed while a larger area is obtained when compared to the manual layout.

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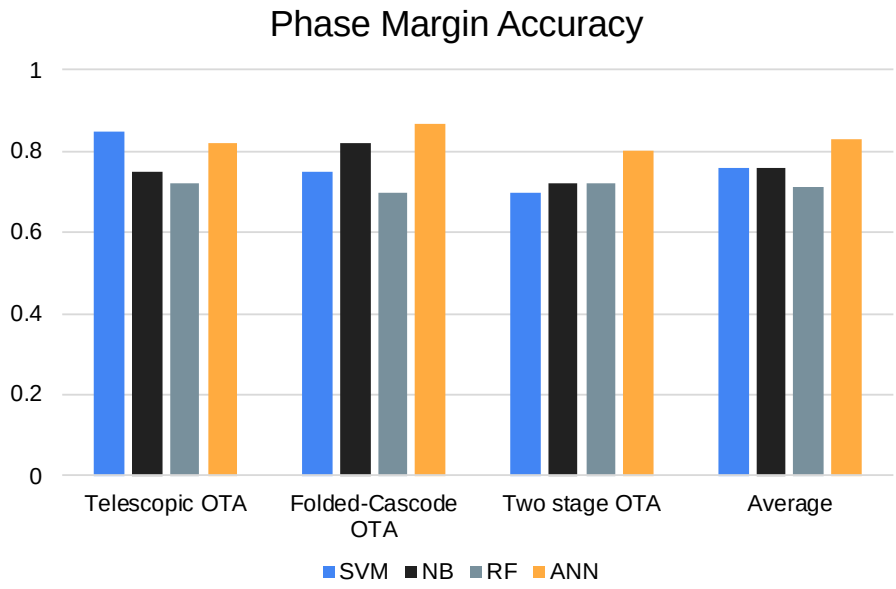

Figure 5. Machine Learning Model Phase Margin Accuracy

5. Conclusion

A machine learning technique based guided analog IC placement model driven by performance factor is proposed in this paper. During the preparation of training data for machine learning model, the layout design is avoided largely in this model. Along with accuracy, fidelity of the model is also analyzed. The proposed approach outperforms traditional automated systems in terms of performance, as evidenced by the experimental findings. In addition, when compared to the manual arrangement, the circuit performs nearly identically with a small improvement. Multiple machine learning approaches are compared and their performance is analyzed for three different types of OTA circuits. Several other analog circuits maybe applied with machine learning models to test the performance in future research.

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