Recent Research Reviews Journal (ISSN: 2583-7079)
https://irojournals.com/rrrj

A Detailed Analysis of Wafer Scale Integration and Multichip Modules

P. Hengjinda

Department of Industrial Robotics and Automation System, Phetchaburi Rajabhat University, Phetchaburi, Thailand.

E-mail: pisith.hen@mail.pbru.ac.th

Abstract:

Hybrid integration of functional multichip layers and electronic devices has received a significant research interest from both industry and academia. While moving towards the end of Moore's law, the power consumption and device scaling remain as significant challenges, necessitating the development of beyond-multichip technologies to achieve high performance computing. While conventional techniques like wafer based bonding and pick-and-place can only partially address the aforementioned challenges, a variety of new multi-chip transfer and wafer scale circuit integration approaches have been developed. This review summarizes such wafer scale integration and neural networks based on multichip modules for many applications, such as flexible electronics, smart displays, and gaming. The proposed study has showcased a wide range of multi-chip modules, and the need for wafer scale integration with expanded functionalities. Finally, a detailed analysis on the advantages of the state-of-the-art techniques has been provided and the future research directions are discussed.

Keywords: Multi Chip Modules (MCM), hybrid integration, wafer based integration, high performance computing

1. Introduction:

Multi-chip materials, circuits, and packages continue to serve as the foundation for the majority of modern integration circuits and electronics. Needless to say, electronic components can be found almost anywhere, from large TVs, smart cars to modern computers. They have made a significant impact on our daily lives [1]. Doped technology advancements have resulted in the formation of high-quality silicon layers on specific substrates. In a Multichip Module (MCM), multiple circuits and devices are embedded and combined into a single kit. The MCM

DOI: https://doi.org/10.36548/rrrj.2022.1.007
© 2022 Inventive Research Organization. This is an open access article under the Creative Commons Attribution-Non-commercial International (CC BY-NC 4.0) License

could be used instead of the traditional Application Specific Integrated Circuit (ASIC) technology [2]. When compared to ASIC, it is a viable option with lower cost and time, and with an increased reachability. It offers numerous benefits, including a significant increase in integrated circuit efficiency by replacing multiple chip board with a single board.

Especially in semiconductor devices, the growth substrate will usually be preserved soon after the completion of chip fabrication [3]. Also there are different situations where the layers of the semiconductor should be very thin and also in some particular situation, it should be transferred to another substrate by removing the transfer layer. For e.g.: the utilization of GaN based LED chips in general lighting applications. But it is well-known that GaN based LED has poor heat dissipation properties. The multi-chip interconnection using wafer scale integration are accompanied by incorporating metal etching or photolithography process [4]. However, none of the existing technologies offer a formidable wafer as combination of multichip modules and micro matching of the packed integrated circuitry. Furthermore, the existing technologies also suffer from reduced yield, low accuracy in circuit alignment, and poor robustness [5].

The recent development of wearable electronic devices is the major driving force for developing a cost-effective wafer scale integration. Henceforth, heterogeneous interconnection of multiple layers and different chip components into a single wafer-level substrate will remain as a major driving force for modern electronics.

2. Multichip Module

With every new generation of IC, the circuitry becomes denser and functionally complex. This makes the existing hybrid multichip based circuit as multichip module. Basically, MCMs are referred as hybrid microcircuit extensions with higher degree of density (for instance: 30% higher silicon to substrate density) to deliver enhanced electrical characteristics and performance [6].

Based on the interconnected substrate, totally there are three basic types of Multichip Modules:

1. MCM_D: This type has an interconnected substrate using thin film with deposited dielectrics and conductors using the process of photolithography.
2. MCM_C: This type has an interconnected substrate using thick film with multi layers and ceramic tape in a singular monolithic structure.

3. MCM_L: This type has an interconnected substrate using organic/plastic laminate with an over moulded outer laminated structure.

The other types and characteristics of Multichip Modules (MCMs) are mentioned in Fig. 1 & Table 1 respectively.

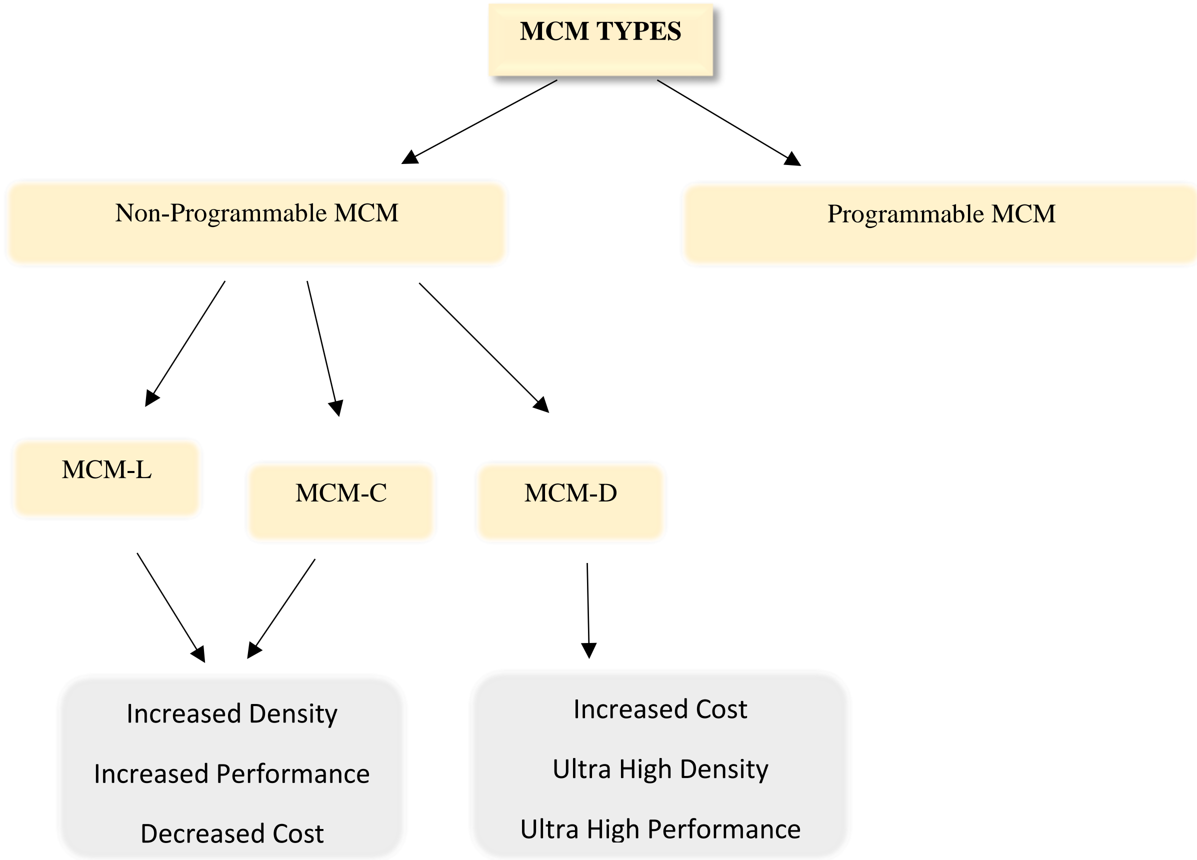

Figure 1. Types of Multichip Modules

Table 1. Characteristics of Multichip Modules

Characteristics	**MCM-D**	**MCM-L**	**MCM-C**
Line Width	10	750	125
Line Density	>400	250-400	200-400
Turnaround Time	10-20 Days	9-12 Weeks	1 Month
Availability Period	5-6 Years	45-50 Years	10-11 Years

Some notable advantages of MCMs are [8]:

1. Enhanced performance with reduced interconnection length
2. Compactness
3. Enhanced reliability
4. Fast market reachability
5. Flexibility
6. Reduced crosstalk and capacitance loading
7. Reduced capacitance and electric supply inductance
8. Simplified design

3. Wafer Scale Integration

In the basic process of electronic chip manufacturing, a memory, processor, or other electronic circuits of computer chip are printed onto a thin silicon disc known as a wafer. A wafer is indeed a sphere with a diameter of about 12 inches today. A chip is a square shaped element with a side length of less than an inch. Upon that wafer, many versions of the same chip can be printed. This will then be arranged as a grid with scribe lines connecting them as shown in Fig. 2. Wafer-scale integration is the concept of creating a single chip from the entire wafer [10].

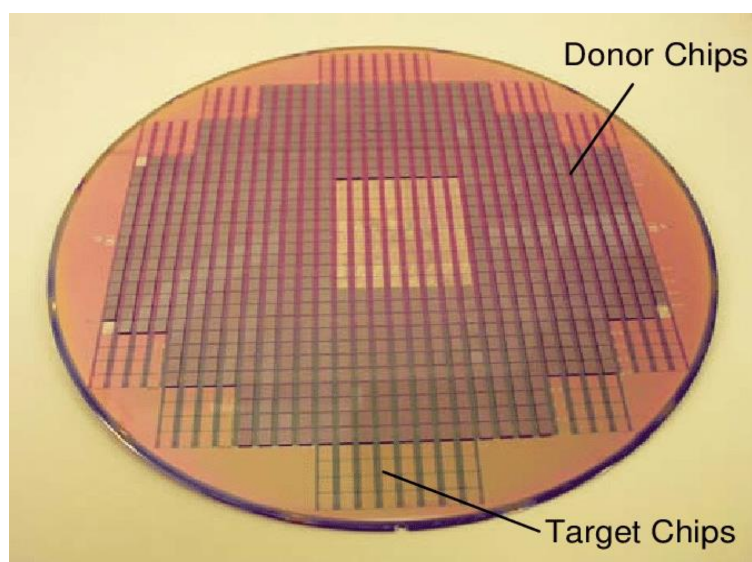

Figure 2. Wafer Level Chip processing [9]

All benefits of high-end MCMs should be possible with wafer scale integration. Extremely compressed packaging should be possible by maintaining the chips implanted in the wafer and assembling all inter-chip routing as a part of the chip's multilayer metalizing architecture. This does not require any additional assembly. However, the significant challenges with this approach are cost and yield.

Figure 3 depicts the factors that influence the optimal size of a wafer die. Lower cost per gate attained by the mask level integration of transistors is highly efficient than assembling the electronic components sliced from a wafer. However, the increasing number of gates, decreases the yield and as a result the cost per function increases unprecedently. The optimal wafer die size for balancing integration and also the yield gets increasing constantly [7].

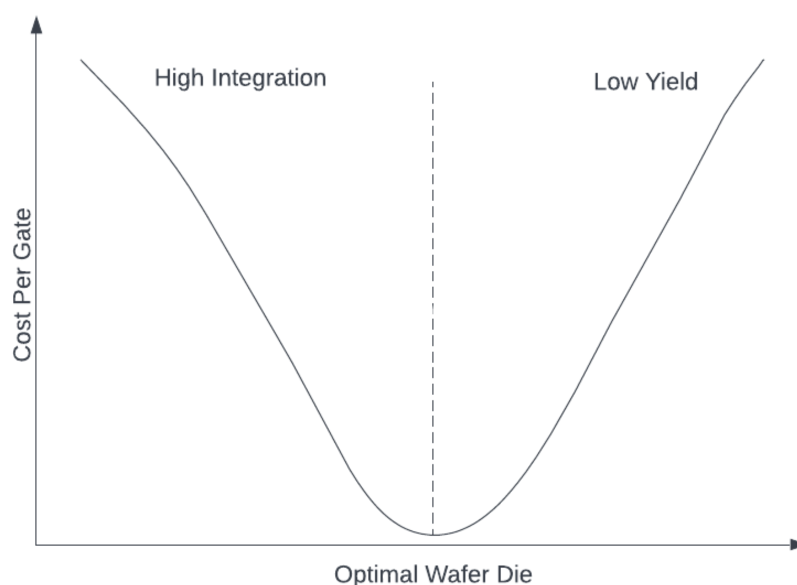

Figure 3. Wafer Scale Integration Trend

When compared with memory wafers, random inference wafers present significant challenges for wafer design, particularly when self-testing, redundancy, and self-rerouting are involved. On-chip packet switching of large gate arrays currently necessitates 4-6 layers. A high-density WSI wafer may require 9 to 10 layers in total. Since the value of a good wafer at the 8th or 9th layer is very high, the final interconnect will result in extremely high yield.

To confront the prospective density of wafer scale integration, a cost-efficient strategy is implemented to always utilize the optimal size die and reconstruct wafer. This approach is referred as wafer scale reconstruction that enables multichip modules.

4. State-of-the-art Technologies

Recently, Schemmel et al., [11] have incorporated Artificial Intelligence (AI) technology in the process of wafer scale integration. Here, Artificial Neural Network (ANN) model has been incorporated to develop a programmable topology. This technique has resulted in reduced power consumption with enhanced fault tolerant model and advanced transferability. Further, Khosla et al., [12] have simulated the LASER based interaction by processing advanced materials. This has highly assisted in providing an advanced coating for next-generation electronic devices along with denser films and adherent coatings. Giambra et al., [13] have designed the novel three-stage protocol for Graphene driven photonic devices in order to enable wafer-scale based complete process flow. Liu et al., [14, 15] developed an AU assisted exfoliation process to realize monolayer wafer-scale MoS_2 with appropriate thickness, high uniformity & grain size, and reduced defects. Further, they have extended the work by developing a wafer level yield using the damascene process to leverage ultra-low dispersion and eliminate the trade-off between the surfaces etch and roughness.

Yuan et al., [16] have designed a wafer-level glass and multichip scale package for enhancing three most significant reliable designing parameters such as PI thickness, die and glass. The developed chip level package also assisted in enabling intrinsic and extrinsic prediction capability by minimally utilizing the training dataset. This package can also be applied in sequential artificial neural networks that require finite element modeling. Guo et al., [17] have additionally incorporated a chemical reaction and evaporation mechanism to support the implementation of vapor cells fabrication in MEMS application. The major advantage of this mechanism is that it highly satisfies the CSACs requirements by avoiding the risk of contamination.

Bloaicher et al., [18] have proposed a hybrid mechanism for photonic integration in order to implement 3D based nano printing mechanism in the domain of optical waveguides. With its simplified assembly, it plays a potential role in the design and development of advanced multi-chip systems. The real-time application of this technology includes designing the transmitter modules for the high-speed telecommunication systems. Quellmalz et al., [19] have designed a large-scale wafer based integration in 2D material with wafer adhesive bonding. This method helped to establish a successful transfer of 2D materials from the initial growth substrate to the final target wafer. Kampasi et al., [20] have dedicated a significant research contribution towards the process of advanced wafer-scale micro fabrication and micro

packaging. This technique helped to implement advanced high resolution micro fabricated wafer-scale based material. This material can be used in the developing minimally invasive imaging and optical waveguide applications.

Table 2: Comparison of various existing techniques

S.no	Reference	Technique	Applications	Outcome	Advantages
1	Schemmel et al. [11]	Artificial neural network for wafer-scale integration	VLSI implementations	Wafer-scale ANN with programmable topology	1. Power consumption. 2. Fault tolerance and the transferability.
2	Khosla et al. [12]	SLIM (Simulation of Laser Interactions with Materials) based computer modeling	Ultra hard coatings to next-generation photonic, quantum, and electronic devices	Carbon polymorphs fabrication	1. Nucleation sites for diamond growth. 2. Adherent, and denser films. 3. Wide range of coating applications.
3	Giambra et al. [13]	Growth, transfer and fabrication protocols for graphene-based photonic devices	Optical and data communication, Photonics and optoelectronics, Photodetectors	Full process flow for SLG-based photonics on wafer-scale	1. Approach is easier and more reproducible. 2. Higher mobility than polycrystalline films.
4	Liu et al. [14]	AU-assisted exfoliation, CVD, thin film sulfurization, MOCVD.	2D transition metal dichalcogenides	Wafer-scale monolayer MoS_2 realization	1. Desired thickness. 2. Good uniformity. 3. Large grain size. 4. Less defects.

5	Liu et al. [15]	Wafer-scale-yield photonic damascene process	Fabrication technology on wafer level yield	Ultralow-loss, dispersion-engineered Si_3N_4 waveguides exceeding one meter	No trade-off between etch verticality and surface roughness .
6	Yuan et al. [16]	Glass wafer-level chip-scale package	Sequential artificial neural network with finite element modelling	Three key reliability design parameters : Die, glass, PI thickness	Intrinsic and extrinsic prediction capability by utilizing minimal training dataset.
7	Guo et al. [17]	Chemical reaction and evaporation	MEMS vapor cells fabrication	Satisfies sensor requirements such as CSACs	1. Concise and convenient. 2. Avoids contamination risk.
8	Blaicher et al. [18]	Hybrid photonic integration	3D nano-printing of freeform optical waveguides	Simplified assembly of advanced multi-chip photonic systems	1. Transmitter modules for high-speed optical telecommunications. 2. Unlock wide variety of novel applications.
9	Quellmalz et al. [19]	Large-area integration in 2D materials with	Integration of 2D materials in semiconductor	Successful transfer of 2D materials from growth	1. Advancements in fundamental 2D material science.

		adhesive wafer bonding		substrate to target wafer	
10	Kampasi et al. [20]	Micro-fabrication and packaging	Optical implants Cochlear and retinal implants	Advanced wafer-scale micro fabricated material	1. High resolution. 2. Minimally invasive optical waveguide and imaging.

5. Summary, Outlook, and Future Work

The proposed study has summarized different heterogeneous wafer scale integration technologies for multichip systems by implementing multi-chip transfer and wafer layer transfer. Among the discussed technologies, some wafer scale technologies like AU assisted exfoliation and hybrid photic integration techniques, assist in implementing a wafer-scale transfer of multi-chip systems in a cost efficient and intelligent manner without compromising the initial growth substrate of the multichip systems. The wafer-scale integration provides practical ways to design and develop complex functional multi-chip systems, regardless of its original fabrication and growth process. In different cases, such multi-chip systems have faced difficulties in achieving enhanced device performance with extended functionalities by using the conventional circuit assembly technologies. For instance, some of the techniques presented in the proposed review study have overcome the challenges faced by traditional technologies with the advanced techniques such as Artificial Neural Network driven wafer sale integration, simulated LASER based interactions, wafer-scale yield based damascene process, finite element modeling, and micro fabrication technologies.

Despite the significant research progress in wafer scale transfer techniques, there are numerous challenges to overcome, such as the challenges encountered in the field of heat dissipation, quality of the circuit signal, transfer speed, generating large-scale continuous circuits, controlled wafer layer thickness, and handling individual circuits during multi-scale wafer integration. Moreover, the optimization of existing techniques and implementation of new wafer-level technologies would motivate in extending continuous research efforts in the near future.

References:

[1] Wong, C. P., and Michelle M. Wong. "Recent advances in plastic packaging of flip-chip and multichip modules (MCM) of microelectronics." *IEEE Transactions on Components and Packaging Technologies* 22, no. 1 (1999): 21-25.

[2] Pogalov, A. I., G. A. Blinov, and E. Yu Chugunov. "Structural strength and temperature condition of multi-chip modules." *Russian Microelectronics* 47, no. 7 (2018): 460-464.

[3] Kovacevic-Badstuebner, Ivana, Ulrike Grossner, Dan Popescu, and Bogdan Popescu. "Transient Stability Analysis of Discrete and Multi-chip Power Semiconductor Packages." In *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 391-394. IEEE, 2021.

[4] Ma, Jingyi, Xinyu Chen, Xinyu Wang, Jihong Bian, Ling Tong, Honglei Chen, Xiaojiao Guo et al. "Engineering Top Gate Stack for Wafer-Scale Integrated Circuit Fabrication Based on Two-Dimensional Semiconductors." *ACS Applied Materials & Interfaces* 14, no. 9 (2022): 11610-11618.

[5] Qiu, Yuchen, Bo Zhang, Junchuan Yang, Hanfei Gao, Shuang Li, Le Wang, Penghua Wu et al. "Wafer-scale integration of stretchable semiconducting polymer microstructures via capillary gradient." *Nature communications* 12, no. 1 (2021): 1-9.

[6] Cho, Jun-Dong, and Paul D. Franzon. *High Performance Design Automation for Multi-chip Modules and Packages*. Vol. 5. World Scientific, 1996.

[7] Feng, Yinxiao, and Kaisheng Ma. "Chiplet Actuary: A Quantitative Cost Model and Multi-Chiplet Architecture Exploration." *arXiv preprint arXiv:2203.12268* (2022).

[8] Liu, Guanyu, Ziao Tian, Zhenyu Yang, Zhongying Xue, Miao Zhang, Xudong Hu, Yang Wang et al. "Graphene-assisted metal transfer printing for wafer-scale integration of metal electrodes and two-dimensional materials." *Nature Electronics* 5, no. 5 (2022): 275-280.

[9] Wieland, R. M., P. Ramm, and A. Klumpp. "3D System Integration for high density Interconnects." (2007).

[10] Riley, Parand R., Pratik Joshi, Nayna Khosla, Roger J. Narayan, and Jagdish Narayan. "Formation of Q-carbon with wafer scale integration." *Carbon* (2022).

[11] Schemmel, Johannes, Johannes Fieres, and Karlheinz Meier. "Wafer-scale integration of analog neural networks." In 2008 IEEE International Joint Conference on Neural Networks (IEEE World Congress on Computational Intelligence), pp. 431-438. IEEE, 2008.

[12] Khosla, Nayna, and Jagdish Narayan. "Fabrication of Q-Carbon Nanostructures, Diamond and Their Composites with Wafer-Scale Integration." *Crystals* 12, no. 5 (2022): 615.

[13] Giambra, Marco A., Vaidotas Mišeikis, Sergio Pezzini, Simone Marconi, Alberto Montanaro, Filippo Fabbri, Vito Sorianello, Andrea C. Ferrari, Camilla Coletti, and Marco Romagnoli. "Wafer-scale integration of graphene-based photonic devices." ACS nano 15, no. 2 (2021): 3171-3187.

[14] Liu, Yuchun, and Fuxing Gu. "A wafer-scale synthesis of monolayer MoS 2 and their field-effect transistors toward practical applications." Nanoscale Advances 3, no. 8 (2021): 2117-2138.

[15] Liu, Junqiu, Guanhao Huang, Rui Ning Wang, Jijun He, Arslan S. Raja, Tianyi Liu, Nils J. Engelsen, and Tobias J. Kippenberg. "High-yield, wafer-scale fabrication of ultralow-loss, dispersion-engineered silicon nitride photonic circuits." Nature communications 12, no. 1 (2021): 1-9.

[16] Yuan, Cadmus CA, and Chang-Chi Lee. "Solder joint reliability modeling by sequential artificial neural network for glass wafer level chip scale package." IEEE Access 8 (2020): 143494-143501.

[17] Guo, Ping, Hongling Meng, Lin Dan, and Jianye Zhao. "Wafer-Level Filling of MEMS Vapor Cells Based on Chemical Reaction and Evaporation." Micromachines 13, no. 2 (2022): 217.

[18] Blaicher, Matthias, Muhammad Rodlin Billah, Juned Kemal, Tobias Hoose, Pablo Marin-Palomo, Andreas Hofmann, Yasar Kutuvantavida et al. "Hybrid multi-chip assembly of optical communication engines by in situ 3D nano-lithography." Light: Science & Applications 9, no. 1 (2020): 1-11.

[19] Quellmalz, Arne, Xiaojing Wang, Simon Sawallich, Burkay Uzlu, Martin Otto, Stefan Wagner, Zhenxing Wang et al. "Large-area integration of two-dimensional materials and their heterostructures by wafer bonding." Nature communications 12, no. 1 (2021): 1-11.

[20] Kampasi, Komal, Ian Ladner, Jenny Zhou, Alicia Calónico Soto, Jose Hernandez, Susant Patra, and Razi-ul Haque. "POEMS (Polymeric Opto-Electro-Mechanical Systems) for advanced neural interfaces." Materials letters 285 (2021): 129015.

Author's Biography

Pisith Hengjinda received his B.S. and M.S. degrees in electrical engineering from King Mongkut's University of Technology Thonburi (KMUTT), Thailand, in 2012 and 2014, respectively. He is currently pursuing a Ph.D. degree in the Department of Electrical Engineering at Da-Yeh University (DYU), Taiwan. He has been a lecturer at Phetchaburi Rajabhat University (PBRU), Thailand. His research interests are in AI technologies, robotics, microcontrollers, and sensors.