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Energy-Efficient Neuromorphic Architectures Enabled by Resistive Memory

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Abstract

Their excellent performance and compatibility with CMOS technology, while the OXRAM (Oxide-based CMOS Resistive Random Access Memory) technique used in CMOS transistors presents challenges in terms of device unpredictability and scalability, also offers potential advantages such as higher endurance, lower power consumption, and quicker reading and writing operation speeds when compared to traditional Flash memory. The inability of conventional SRAMs to store data after powering off limits their use in battery-operated mobile devices and other applications where non-volatility related to zero leakage currents is required. In the article, a new OXRAM-based Non-Volatile SRAM (NVSRAM) device is presented. It is suggested to compare the performance of SRAM with NVSRAM at the memory and cell levels. Learning is crucial for the brain's ability to adapt to changing conditions. A synaptic connection table in an external memory at a local routing node is used to learn a rule in the address domain for neuromorphic architecture. A number of parameters are compared, including design complexity, leakage current values (SRAM cells are 3.4µA, 7.4nA) and (NVSRAM-based OXRAM are 2.7 µA, 5.9nA) at 180nm and 90nm, and energy saving or power usage values (SRAM cells cell are 5.5 µA, 10.5nA) and (NVSRAM based OXRAM are 4.9 µA, 9.8nA) at 180nm and 90nm. The circuits that are being described can be realized using far-above ground voltage CMOS Cadence tools at 180 nm and 90 nm.

Keywords: Static Random CMOS Access Memories (SRAMs), Non-Volatile CMOS SRAM (NVCSRAM), OXRAM, Power Dissipation, Technology

1. Introduction

The construction of low-power devices, with an emphasis on integrated photonic components, is becoming more critical as lightweight computers become more popular and IoT systems more complex. These devices offer high-speed, power-efficient photonic acceleration solutions, thus providing a promising alternative to digital circuits [1, 2]. Multiple studies have aimed at enhancing optical structures, particularly the efficiency of photodiodes and information converters [3]. Yet, a compelling desire remains to create reliable, low-energy memories for such systems [4, 5].

A few neurological devices based on SNNs have been designed for AI purposes. Since SNNs utilize pulses as signals for neuromorphic computation, they are closer to actual biological neural networks compared to conventional ANN, or artificial neural networks, SNNs

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significantly enhance parallel computing performance by representing information transmission in the form of temporal relationships between spikes. Low-power neural computing functions are expected to benefit significantly from brain-inspired SNNs [6-7].

The persistent "von Neumann bottleneck" has stimulated the search for novel approaches to computation that can address the increasing demands of data-intensive and low-cost applications. Neuromorphic computing, which mimics the brain's highly efficient and low-power consumption, has been a promising substitute. Original neuromorphic hardware demonstrated the potential of this method, but new breakthroughs in hardware, particularly in memory developments, have accelerated the maturity of the field. In particular, with the advent of technologies such as Resistive Random-Access Memory (RRAM), the groundwork for building more scalable and efficient neuromorphic hardware has been well established, leading to applications ranging from low-power edge computing to wearable AI. Though various works have provided an overview of neural computation and its basic principles, most focus either on cutting-edge architectural concepts or on explicit device-level physics.

There exists an essential gap in the literature for a targeted work that correlates the development of new memory techniques, like combination non-volatile SRAM (NVSRAM) and RRAM, with the architectural considerations of Spiking Neural Networks (SNNs) for existing applications. For instance, a detailed investigation into how different memory-processor integration schemes influence the power efficiency of SNNs for edge AI remains missing. This survey makes up for the gap by providing an extensive analysis of modern neuromorphic designs, emphasizing the role of novel Non-Volatile memory (NVM) devices. In order to evaluate architectural performance, we present an extensive analysis of interactions between memory technologies, SNN models, and the system-level architecture.

Our primary contribution is to integrate existing findings to present a novel perspective on how developments in memory-device technology are impacting neuromorphic systems of the next generation that are being used in power-constrained applications like edge computing. This work proposes a groundbreaking OXRAM-based NVSRAM architecture that combines OXRAM and CMOS technologies to enhance reliability and performance. Through the application of SRAM constituents to compensate for OXRAM's natural fluctuations at real operational times, the design effectively addresses unpredictability without being volatile. The proposed architecture is more energy efficient compared to conventional SRAM at 180nm and 90nm nodes. At the 180nm node, it has low leakage current (2.7 μA compared to 3.4 μA) and power.

2. Analysis of the Proposed Cell Methodology

2.1 9TSRAM Cell

Figure 1 depicts the working concept of typical 6T SRAM cells with 180nm and 90nm CMOS semiconductor sizes. Figure 2 illustrates the usual architecture of a 6T SRAM cell. The word line (WL) controls the two accessible barriers (NM2 and NM3), which define where the cell needs to be linked through the bit lines (BL and BLB), making the cell available.

Both the read and write procedures use them to convey data. Even if an additional pair of bits per line is not required, providing both the input signal and its inverse typically boosts noise margins. Using this architecture, data stability improves while leakage power decreases. During the reading process, the 9T SRAM cell completely isolates the data from the bit line.

Unlike ordinary 6T SRAM cells, idle 9T transistors are placed in a super cutoff stage of deep sleep, reducing leakage power consumption. Figure 3 depicts the schematic for 9T SRAM cells. The 9T SRAM cell experiences either static or dynamic power dissipation; however, the architecture is especially designed to lower both when compared to previous 6T cells. A notable benefit of the 9T architecture is the complete separation of nodes storing data during read operations, which considerably reduces dynamic power usage during reads.

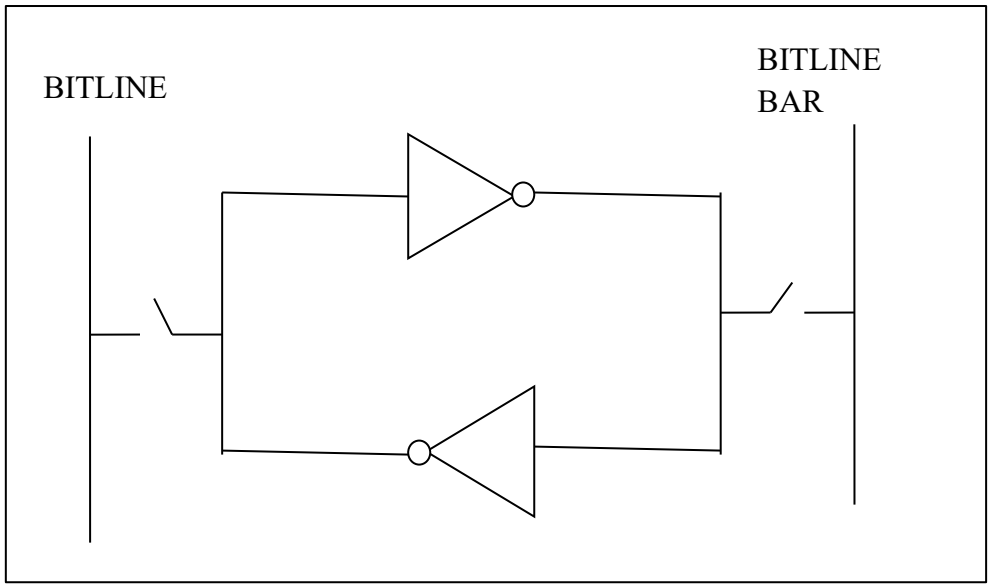

Figure 1. Operational Concept of SRAM Cell

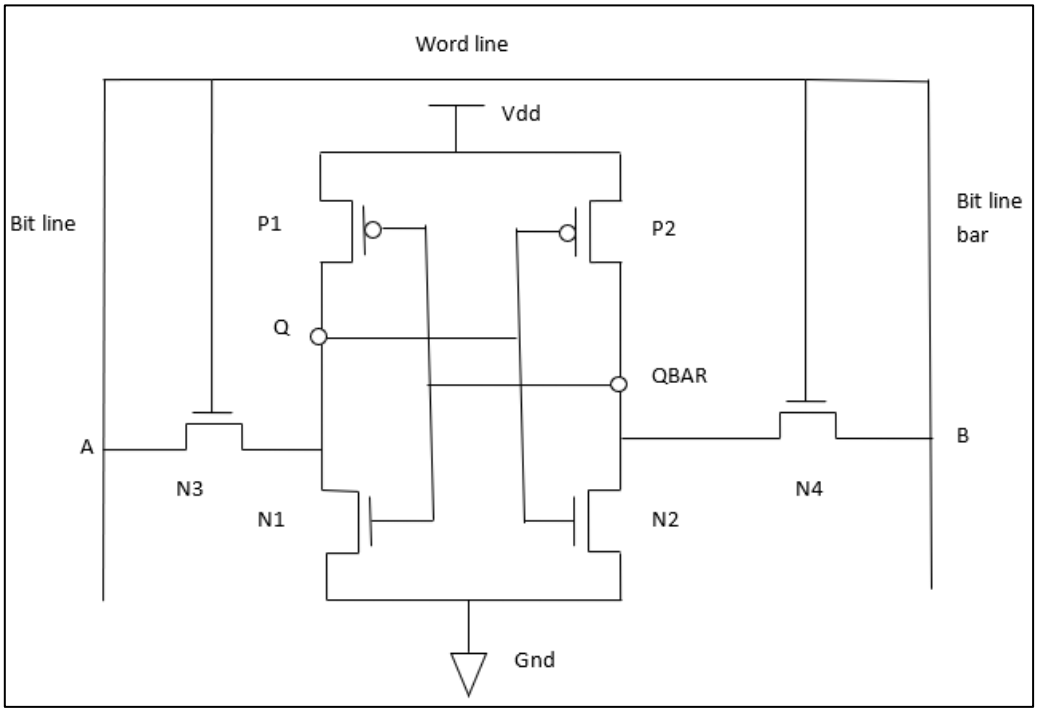

Figure 2. Standard Architecture of 6T SRAM Cell

The inverters serve as storage elements, reinforcing each information bit throughout the cell as long as power is available (VDD). PM0 and PM1 are PMOS transistors; NM0, NM1, NM2, and NM3 are NMOS transistors. NM2 and NM3 are the access semiconductors (or pass transistors) that connect the cell to the Bit Lines (BL and BLB).

The write signal (WL) controls the two accessible write transistors (NM2 and NM3). The data is stored in this top memory sub circuit. The lower sub circuit of the new cell is made up of data line accessibility semiconductors (NM4 and NM5) and an access for reading transistor (NM6). The data contained in the cell (Q and QBAR) controls the activities of NM4 and NM5. NM6 is regulated by an additional read signal (RD).

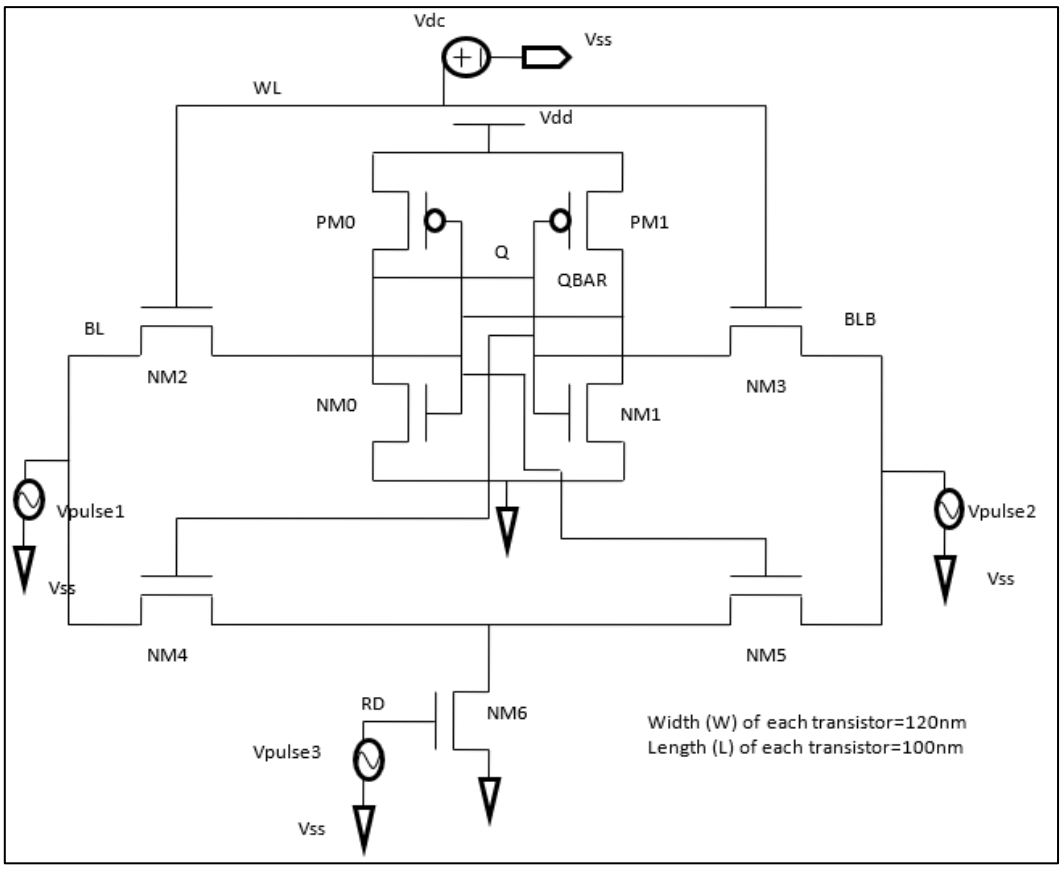

Figure 3. Diagram for a 9T SRAM Cell

2.2 OXRAM Technology

A physical model that predicts OXRAM variation during the Low Resistance Phase (LRP) and High Resistance Phase (HRP) is described. The purpose of this investigation is twofold. Variability is, in fact, one of the problems preventing OXRAM technology from being widely used in commercial products from the perspective of traditional memory applications. Therefore, advice to lessen this problem may be provided by studying the source of OXRAM resistance fluctuations. From the perspective of neuromorphic computing, OXRAM devices are a perfect fit for artificial synaptic implementation. Studying the effects of synaptic variability at the system level can be accomplished by creating a model that can replicate device variability under a variety of programming circumstances.

In addition to their typical physical structure, two basic switching states the OFF and ON states, associated with the conductive filaments (CF) of the RRAM devices are commonly characterized electrically. Low-resistance-state (LRS) and high-resistance-state (HRS) are other names for these states, respectively. By changing resistance states, RRAM devices may complete the data storage function based on "0" or "1". The device's LRS value shows a high conductance state, whereas its HRS value shows a low conductance condition. The ratio of HRS to LRS determines the ON/OFF ratio.

The SET action is defined as the transition from HRS to LRS by means of the functional voltage bias, and the RESET function is the transfer from LRS to HRS. VSET and VRESET are the stop voltages for the SET and RESET processes, respectively. Unipolar and bipolar switching are often classified as two distinct kinds [8], as shown in Figure 4. The bipolar mode of switching is determined by the orientation of the voltage that is used for bias, whereas the unipolar switching mode is determined by the frequency range of the supplied voltage bias.

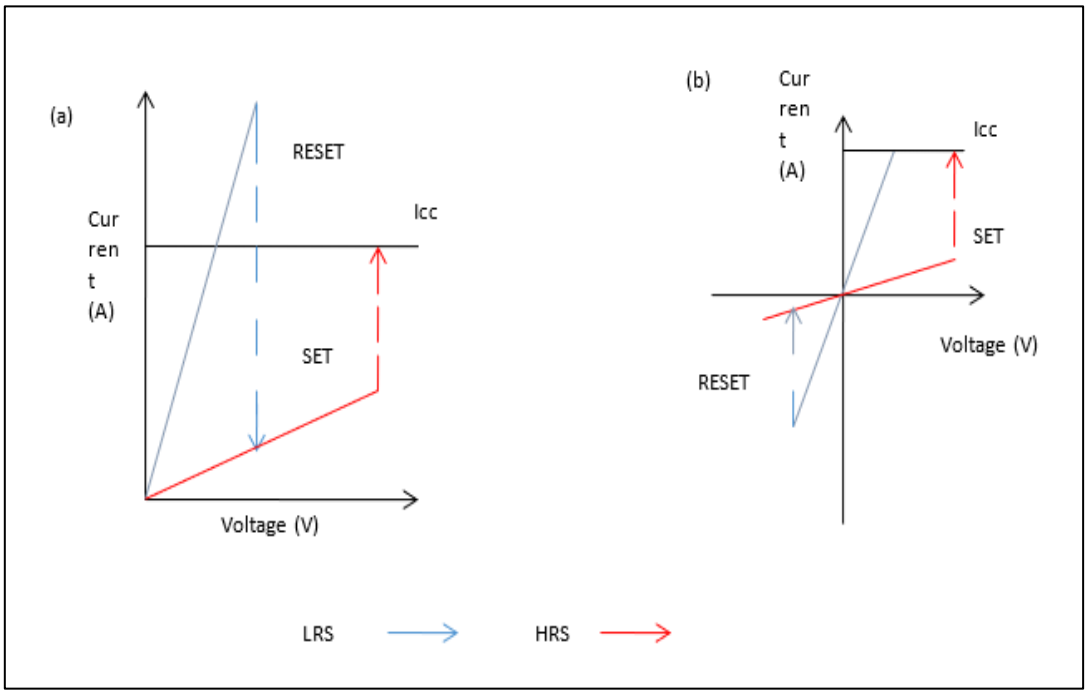

Figure 4. (a) SET/RESET Unipolar RRAM Devices and (b) SET/RESET Bipolar RRAM Devices

Modeling oxygen vacancies in an insulator layer depends on an induced electric field that creates and destroys them. Constantly monitored procedures to transition between high and low resistive states are handled by a unique equation that governs the resistance of each filament. The following solutions are given in equations (1) and (2):

$$\frac{dr_{cf}}{dt} = (r_{CF}max - r_{CF}) \,.\, 10^{\beta_{redox}} \,.\, e^{-\frac{Eo - qr_{ed} - vcell}{kb - t}}$$

(1)

$$-r_{CF} \,.\, 10^{\beta_{redox}} \,.\, e^{-\frac{Eo - qr_{ed} - vcell}{kb - t}}$$

Here, the red oxide reduction rate (RedOx), the activation energy (Ea), the transfer coefficients (ranging from zero to one) of red and orange, and the Boltzmann constant, rCFmax,

represent the maximum diameters of conductive filaments. Various assumptions, such as a homogeneous electric field and a finite filament radius, are included in the model. Several factors affect how quickly a response occurs, including temperature and time of day. To sum up, the OXRAM total current consists of a conductive current (ICF) and a conductivity-related current (OCR) (IOX). The following are the formulas for ICF and IOX:

$$I_{CF} = \frac{V_{cell}}{L_x} . (\pi . r_{CF}^2 . (\sigma_{CF} - \sigma_{OX}) + \pi . r_{CF}^2 max . \sigma_{OX}) \quad (2)$$

Oxidation and reduction rates are represented by Ox and CF respectively. The oxide thickness, SCell, is determined by Lx. Therefore, IOCX catch enhanced contemporary capability by examining two constraints, ACHRS and HCRS associated with the power-law between the bias provided and group currents. To sum it up, the cell's total current flow is represented by the following equations (3) and (4):

$$I_{OX} = A_{HRS} . S_{cell} \left(\frac{V_{cell}}{L_X}\right)^{\beta_{HRS}} \quad (3)$$

$$I_{cell} = I_{CF} + I_{OX} \quad (4)$$

2.3 9T NVSRAM Storage Unit

The suggested 9T configuration is shown in Figure 5. Compared to the most advanced NVSRAMs, this new cell contains fewer control signals. The typical access transistors NM2 and NM3 are coupled to the OXRAM PX0 and PX1 devices. Other transistors called NM4 and NM5 are employed for the STORE and RESTORE non-volatile storage functions. The two operations that make up STORE are SET and RESET. In the OXRAM device, SET writes "1" and RESET stores "0."

WL and BLB are placed near the ground during FORMING, whereas BL and WL are placed far above the ground. The OXRAM may be created in a single step at this point (NM4 is ON: BL and the OXRAM are directly connected). BLB is grounded, BL is set to 0.7 V, and WL is pulsed to set in motion the access transistors (NM2 and NM3). A WRITE process comes before a STORE operation. WL and BLB are placed far above the ground and BL and WL are place near the ground during the WRITE "0" operation. Following WRITE "0," RESET is the step where WL and BL are placed near the ground. BLB and BL are pre-charged to VDD/2 (0.7V) during the Precharge step. READ operations are often carried out via WL, which is placed far above the ground. Each of the indication, including VDD, is switched off following storing (SET and RESET) and READ operations. To keep the data when the power goes out, the RESTORE process is necessary. WL is placed far above the ground and Vdc is enabled in order to complete RESTORE. We keep all other signals low. After RESTORE, Precharge and READ proceed as usual, with WL set high and low at the same time.

A schematic of the 9T NVSRAM is shown in Figure 6. The transistors NM4 and NM5 are coupled to the OXRAM PX2 and PX3 devices. BL and BLB are precharged to Vdd/2 (0.7V) during the precharge step. Reading operations (RD) are often carried out via WL, which is placed far above the ground. Every single one of the indications, including Vdc, is switched off following the storing (SET & RESET) and reading functions. To keep data when the power goes out, the RESTORE process is necessary. WL is placed far above the ground, and Vdc is enabled in order to complete RESTORE. We keep all other signals low. After RESTORE, precharge and READ proceed as usual, with WL set high and low at the same time.

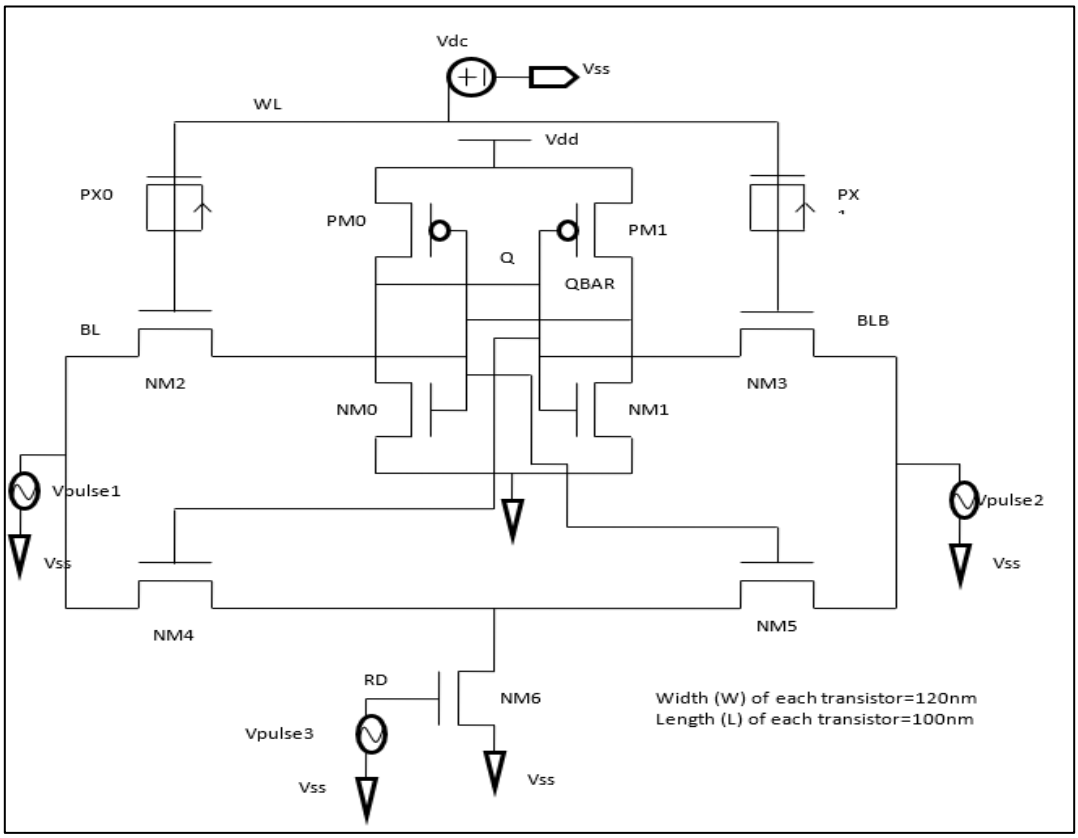

Figure 5. Schematic of 9T NVSRAM (PX0 and PX1OXRAM)

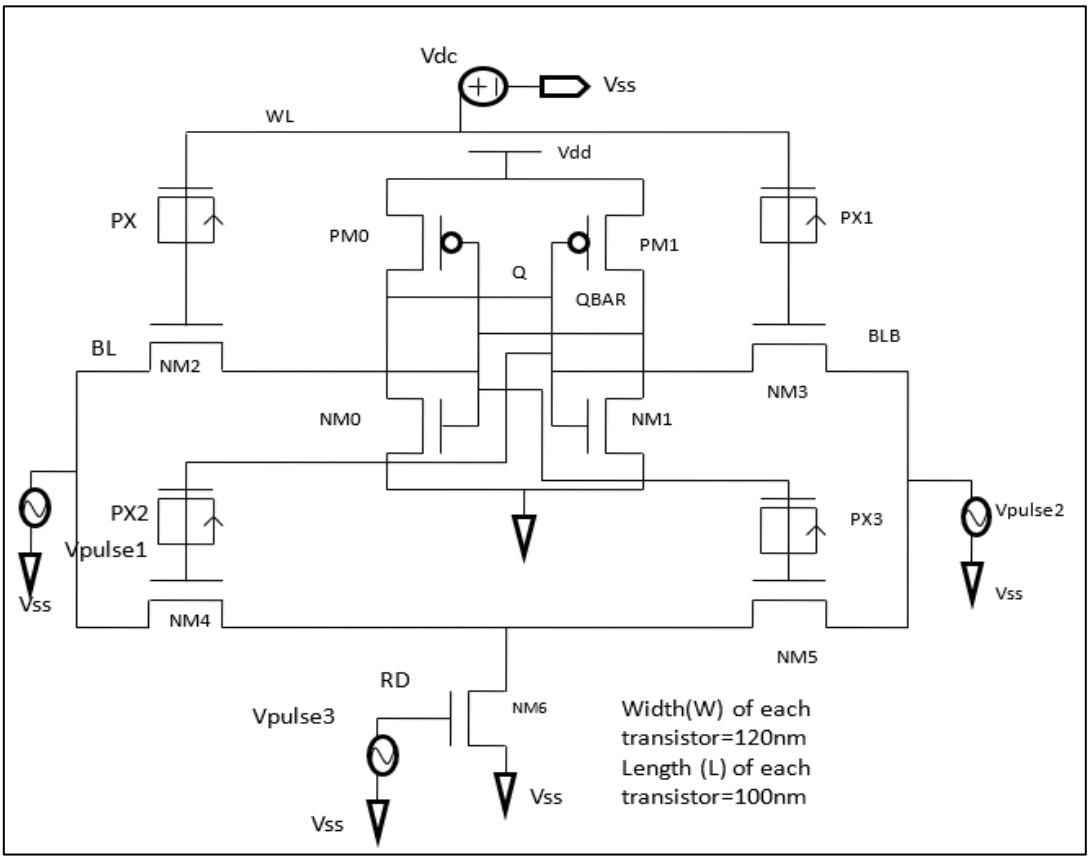

Figure 6. Schematic of 9T NVSRAM

2.4 Synaptic Configuration and SDSP Training Model

After presynaptic voltage signal pulses are converted by synaptic transmission, postsynaptic currents, which are controlled by synapse weight, are delivered into the membrane of the target neuron. Since synaptic weight theoretically transforms brief presynaptic pulses into persistent postsynaptic currents with intricate temporal dynamics, linear exponentially temporal features facilitate this process. In Very LargeScale Integration (VLSI) technology SNN (VLSI technology) SNNs designs, currents from several synapses are combined in a single postsynaptic neuron circuit. Postsynaptic potentials rise with higher excitatory activity in synapses and fall when there is greater inhibitory activity due to the weighted average of information from the inputs acquired by a postsynaptic neuron.

Therefore, in order to minimize silicon surface area and ensure optimal synaptic absorption on the chip, synaptic circuits must be small. However, a large amount of silicon real estate may be needed to design synaptic integrator circuitry with straightforward response features and time constants comparable to the membrane time constant of the neuron. Thus, it is a challenging but ongoing task to design small linear synaptic structures that replicate the functional properties of actual synapses. Many designs for synaptic networks have been created that strike a compromise between circuit/layout dimensions, usefulness, and the intricacy of temporal dynamics. Many proposed circuits replicate the biophysical properties of synaptic channels by limiting the signal's dynamic range or including floating-gate devices. Here, we propose properties for synaptic circuits with a wide dynamic range that is linear and exponential.

A synaptic circuit diagram is shown in Figure 7. Excitatory and inhibitory synapses are combined to satisfy SNN criteria with a small design. As a new feature for synaptic circuits, this architecture offers attribute configuration.

A postsynaptic pulse (Pre_spk) and weight (Vw) activate the voltage-controlled sources of current that power the excitatory (NM6–NM7) and inhibitory (NM9–N10) synapses. By using the digital output of Cont to control transistors NM5 and NM8, the synaptic characteristics may be set up to suit real-world requirements. While NM6 creates an excitatory power that is exponentially reliant on the Vsyn endpoints and NM7 modifies the excitatory current's amount via bias voltage Vexc, transistor NM1 serves as a constant current source to the vertically charged capacitor Csyn. To releasing the membrane potentials of neurons, Transistors NM9–NM10 produce an inhibitory synaptic exponential current. The excitatory synapse, for instance, complies with the following dynamics according to the linear transmission principle:

$$\frac{C_{syn}}{I_\tau}\frac{dI_{syn}}{dt} + I_{syn} = \frac{I_w}{I_\tau} \tag{5}$$

WhereI_τ and Iw are currents set by Vt as well as Vw, respectively, and I_synis is the synaptic output current. Current I_τ and capacitor Csyn can be used to alter the synapse time constant. Capacitors must be larger or $I_\tau$current must be reduced in order to raise the circuit's time constant. We modify the aspect ratio of NM1 to provide an ideal exponential current time constant for LIF neurons, avoiding the high area requirements caused by growing capacitance sizes in the 90 nm technology.

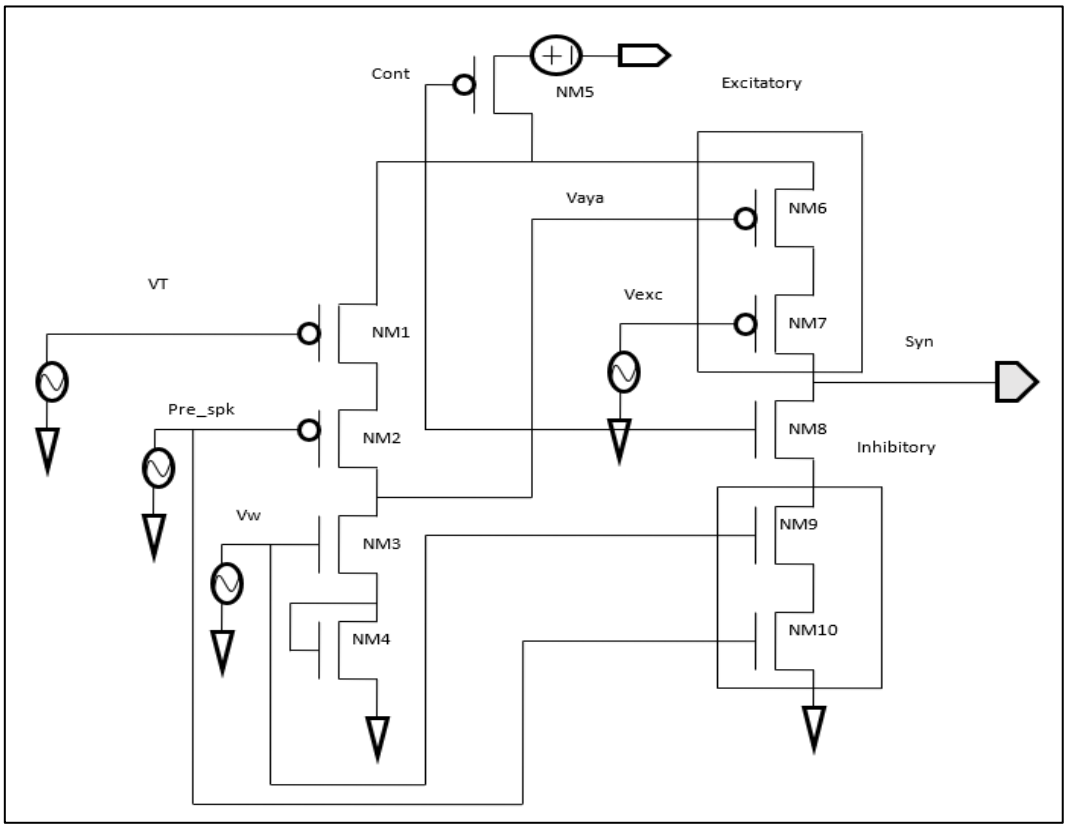

Figure 7. Synapse SDSP (Excitatory and Inhibitory) Circuit Schematic

Neuromorphic hardware design techniques have been compared by Frenkel et [9]. The term "bottom up" refers to neural and synaptic modeling that replicates the biological mechanism in silico. Examples of its applications include neuroscience research, brain reverse engineering, and hybrid setups between artificial and biological neurons; examples of this type of approach include ROLLS, DYNAPs, BrainScaleS, Neurogrid, SpiNNaker, True North, and Loihi. At the same time, a number of researchers have made improvements that enable the effective to use of SNN for particular tasks that were previously only possible with regular DNN (Liu and Yi [10]. In neuromorphic system design, OXRAM is employed as the synaptic connection table, providing an efficient means of storing and updating synaptic weights. Its use at routing nodes enables localized learning, where adaptation occurs within the address domain, reflecting the brain's natural capability to respond to dynamic conditions. Owing to its fast read/write characteristics, high endurance, and low energy requirements, OXRAM is well-suited to the parallel, low-power computational demands of neuromorphic architectures, making it a promising element for next-generation brain-inspired computing solutions.

3. Results and Simulation

A waveform is a graphical representation of the shape and magnitude of a signal over time. It typically depicts how the voltage of the signal changes over time, with time plotted along the horizontal axis and voltage plotted along the vertical axis. The 9T SRAM waveforms for outputs Q and Qbar are superior to those of others waveforms.

The findings of SRAM and 9T NVSRAM simulations are presented in this segment. In this cell, BL is high and data stored in Q is "0," while and at the same time BLB is low, and

data stored in QBQR is “1” respectively. The transient analysis of 9T SRAM is illustrated in Figure 8, while the leakage current waveform of 9T SRAM units is illustrated in Figure 9. The levels of voltage pulses are adjusted to match the available voltage supply VDD (1.8 and 0.7V).

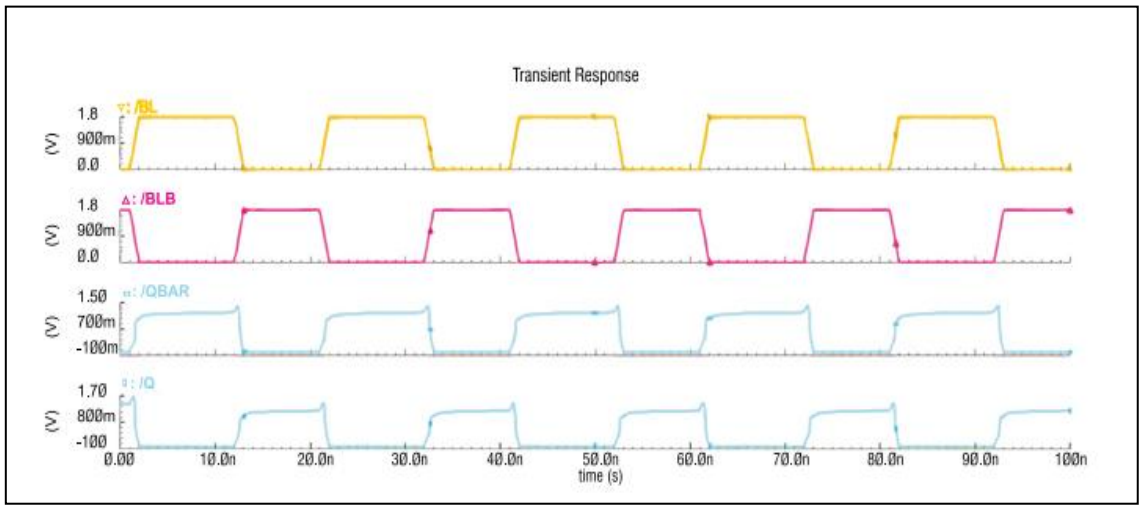

Figure 8. Transient Analysis of 9T SRAM cell

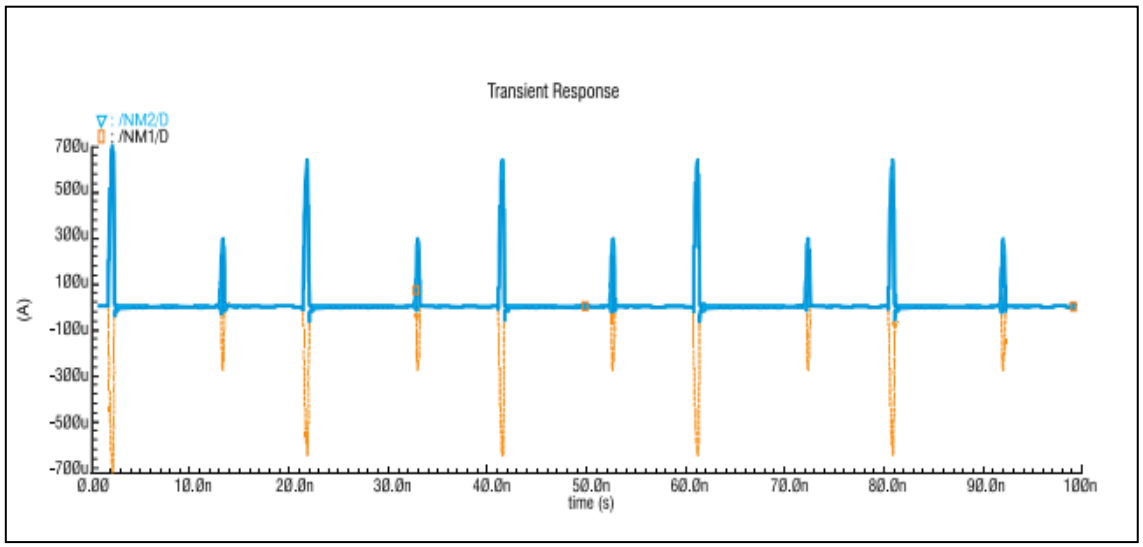

Figure 9. LC waveform of 9T SRAM cell

Transient analysis of the 9T NVSRAM cell OXRAM (PX0 and PX1) is displayed in Figure 10, and the leakage current of the 9T NVSRAM cell OXRAM (PX0 and PX1) is shown in Figure 11, which were produced following the 9T NVSRAM cell OXRAM (PX0 and PX1) simulations. The pre-charge circuit is enabled while pre-charge (the pre-charge indication is "0") and the write drives (WE) and sensing amplifier (SE) are kept off since the selected semiconductor in the pre-charge circuitry is a PMOS. During WRITE, sensing amplifier circuits remain off (SE "0"), while pre-charge circuits are switched off (pre-charge SET high). To access the cells, the write driver is activated (WE "1") when the row's decoding is enabled (ENABLE "1"). To preserve the data inside the cross-coupled inverters, all signals—aside from VDD—are turned off during the HOLD state. When the same conditions of pre-charge from the previous WRITE are satisfied, the following stage is pre-charge before READ. The write drive circuit is disabled, and the pre-charge circuit is deactivated during READ. The BL and BLB sensing pathway may access the chosen sense amplifiers since the column decryption is

maintained ON (ENABLE2 "1"). In one SRAM cell, writing "0" (Q) operation yields the output "0," whereas writing "1" (QBAR) operation yields the output "1."

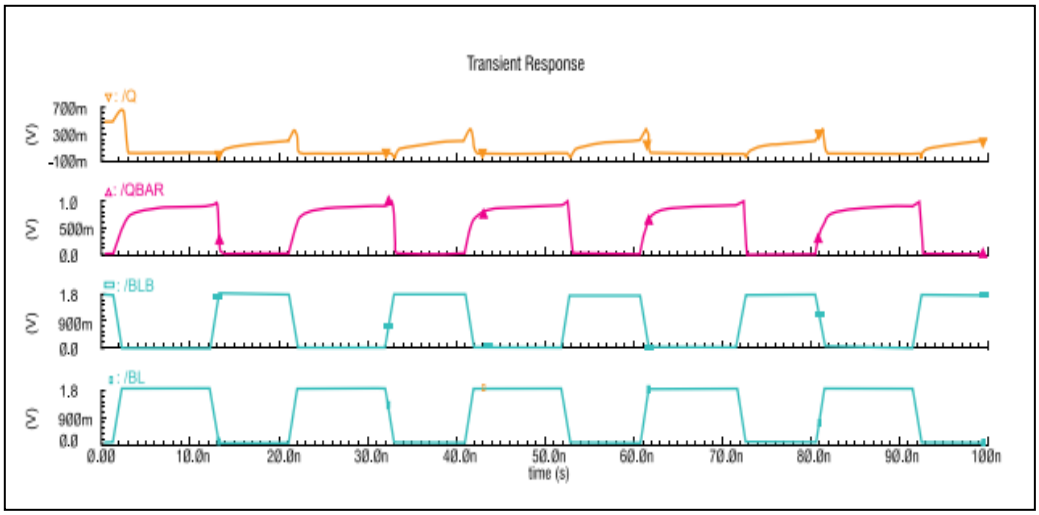

Figure 10. Transient Analysis of 9T NVSRAM cell OXRAM (PX0 and PX1)

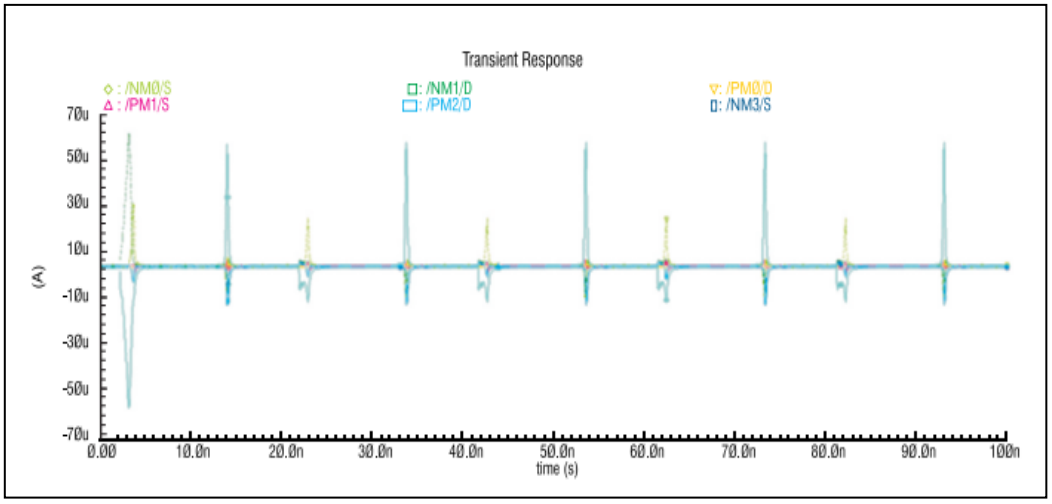

Figure 11. LC waveform of 9T NVSRAMOXRAM (PX0 and PX1)

Figure 12 shows the transient analysis of the 9T NVSRAM cell OXRAM (PX0, PX1, PX2, and PX3). BLB is grounded, and BL is set to 0.7 V. A WRITE process occurs before a STORE operation. BLB is placed far above the ground, and BL is placed near the ground during the WRITE "0" operation. Following WRITE "0," the (Q) RESET step is where BL is placed near the ground. BL and BLB are pre-charged to VDD/2 (0.7 V) during the precharge step, demonstrating low power consumption in the cell. In contrast, Figure 13 shows the leakage current of the same cell.

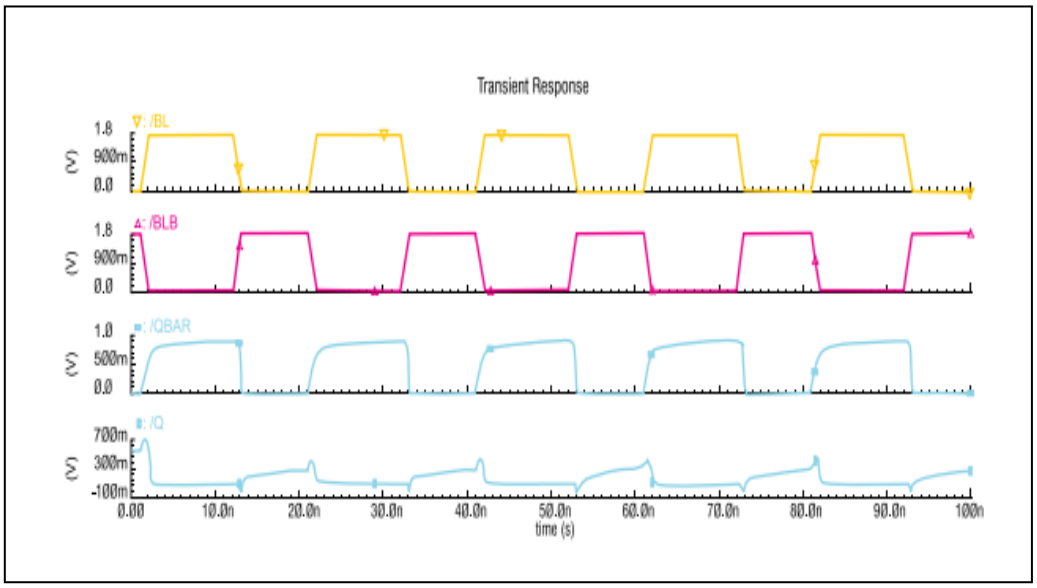

Figure 12. Transient Analysis of 9T NVSRAM OXRAM (PX0, PX1, PX2, and PX3)

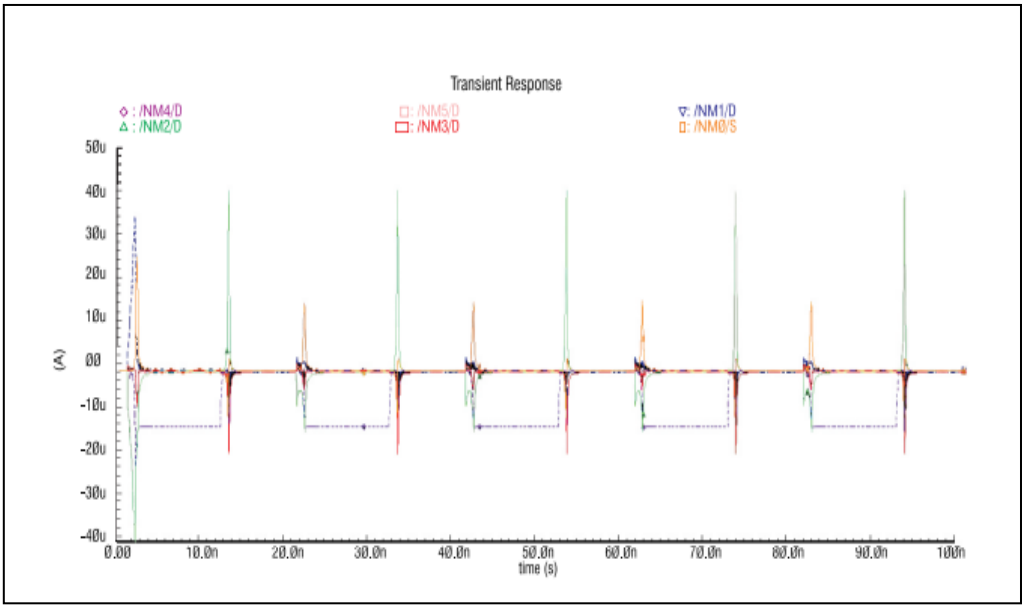

Figure 13. LC waveform of 9T NVSRAM OXRAM (PX0, PX1, PX2, and PX3)

3.1 Performance Parameters of Proposed 9T NVSRAM

This study analyzed a number of cell characteristics and presented a unique 9T NVSRAM cell that was created and simulated using the Cadence tool. The formation of a conducting oxygen film between two terminals determines the OXRAM HRS and LRS. Mobility μv, OXRAM HRS (ROFF), and LRS (RON) have been chosen. The semiconductor film's "D" length is assumed to be 100 nm. The following formula may be used to simulate the linear charge control NVSRAM using two resistors connected in series, as given in the following equations (6) and (7):

$$R(W) = R_{ON} \times \frac{w}{d} + R_{OFF}\left(1 - \frac{w}{d}\right) \quad (6)$$

$$M(Q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON}\, Q(T)}{d^2}\right) \quad (7)$$

Where d is the length of the device, μv is the range of motion of oxygen ions, M (Q) is the overall, and OXRAMRON & ROFF represent the OFF and ON state resistances. A 90 nm Prediction Technology Model scale-up of the technology is used for precise comparison. Various technical nodes' condition parameters for NVSRAM simulation are listed in Table 1.

Table 1. Comparison of SRAM vs. OXRAM-based NVSRAM

Parameter	SRAM at 180 nm / 90 nm	OXRAM-based NVSRAM at 180 nm / 90 nm	Advantage of NVSRAM
Volatile vs. Non-Volatile	Volatile; data is lost when power is off.	Non-volatile; retains data without power.	Enables zero-leakage standby mode and is suitable for battery-powered devices.
Leakage Current	3.4 μA (180 nm) / 7.4 nA (90 nm).	2.7 μA (180 nm) / 5.9 nA (90 nm).	Lower leakage current, especially at the more advanced 90 nm node, leading to significant power savings.
Power Consumption	5.5 μA (180 nm) / 10.5 nA (90 nm).	4.9 μA (180 nm) / 9.8 nA (90 nm).	Lower overall power usage. NVSRAM's zero-leakage standby mode is ideal for low-power applications.
Reading/Writing Speed	High.	Potentially higher for read/write operations compared to traditional Flash memory.	Faster operations contribute to improved system performance.
Endurance	High, but not non-volatile.	Higher than traditional Flash memory.	Longer lifespan and reliability for write-intensive applications compared to Flash memory.
Design Complexity	Conventional SRAM design is a mature technology.	More complex due to the integration of OxRAM components with CMOS.	Higher complexity is a trade-off for non-volatility and lower power consumption.
Scalability	Subject to limitations in CMOS scaling.	Faces challenges with device unpredictability and variability at advanced nodes.	Offers potential advantages at scaled nodes but requires overcoming manufacturing hurdles.

Neuromorphic Application	Requires external memory for synaptic connection tables, leading to increased latency and power.	Can store synaptic connection tables locally, enabling efficient, brain-inspired, low-power processing.	Better suited for neuromorphic computing, allowing for high parallelism and low power dissipation.

3.2 Experimental Result and Discussion

A comparison of SRAM and NVSRAM's power consumption and leakage current is shown in Tables 1 and 2. In normal mode operations, NVSRAM uses a little less power than SRAM, suggesting that both architectures have comparable power consumption when utilized like traditional SRAMs. The OXRAM stores the NVSRAM's data prior to power-off. Definite encoding actions (storing and restoring) must be performed in order to complete this procedure. The NVSRAM cell uses 4.9 µW and 9.8 nW of electricity in this particular instance. Keep in mind that when the power is turned off, the data cannot be saved since the traditional SRAM cell is volatile. VDD is maintained high during the SRAM HOLD state to guarantee data retention. In this state, the SRAM uses between 5.5 µW and 10.5 nW of energy. Table 3 shows the comparison of previous work with 9T NVSRAM-based OXRAM performances, achieving better outcomes. Introducing a new OXRAM-based NVSRAM design. Mitigating unpredictability: By integrating OXRAM with CMOS, the aim is to leverage the best of both technologies, likely using the SRAM component to handle the unpredictability of the OXRAM during active operation. Improving energy efficiency: Comparing the new design against conventional SRAM at 180 nm and 90 nm nodes, with explicit data showing reduced leakage and power usage (2.7 µA vs. 3.4 µA (leakage) and 4.9 µA vs. 5.5 µA (power) at 180 nm). Applying the technology: Demonstrating the relevance of the new NVSRAM for neuromorphic applications by implementing the synaptic connection table learning function in a memory cell. The characteristics of our proposed circuit are contrasted in Table 4 with those of previous programmable circuits used in neuromorphic prosthetic systems [13, 14] and circuitry that follows the same procedure [13]. In contrast to a 180 nm circuit concept [14], our design uses less circuit space and has a higher energy efficiency of 2.52 nJ@50 Hz (Figure 5) than the reference design, which uses 883 pJ@30 Hz. Furthermore, the circuits utilized in [14] & our research follow the same procedure, and it is evident that our design provides notable benefits in terms of both area and power usage.

Table 2. Comparison of 9T SRAM and 9T NVSRAM based OXRAM Performances

Performance Parameter	9T SRAM cell	NVSRAM based OXRAM
Technology	180nm	180nm
Transistor size	W=200nm, L=180nm	W=200nm, L=180nm
Voltage	1.8V	1.8 V
Power consumption	5.5µW	4.9 µW
Leakage current	3.4µA	2.7µA
Delay	24.5µs	23µs

Table 2 results are shown in Figure 14. The graph points out that at 1.8 supply voltage, the values of power consumption, leakage current, and delay decrease with the NVSRAM-based OXRAM technique in comparison to 9TSRAM.

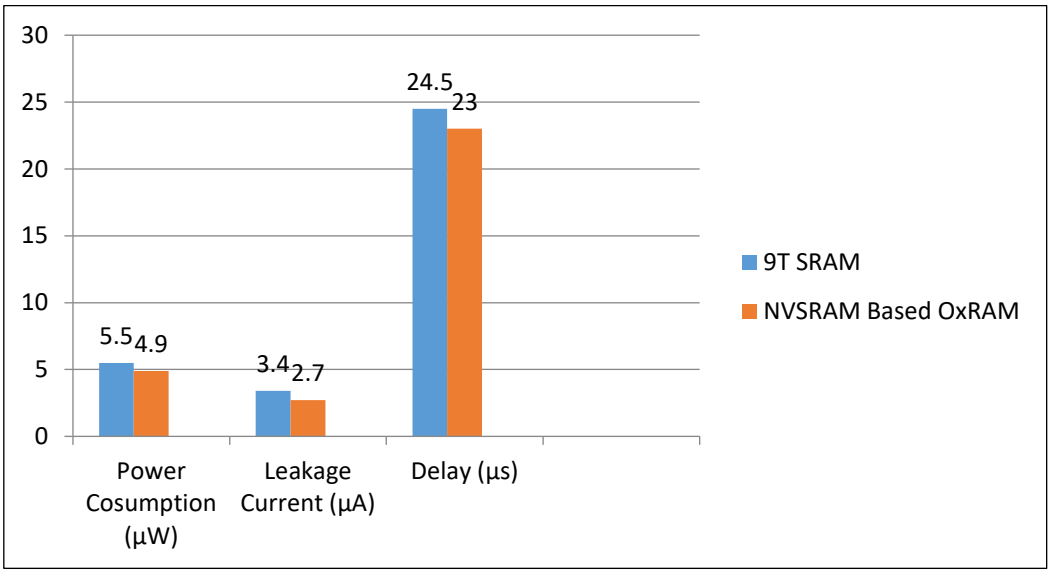

Figure 14. Graph Shows Comparison of 9TSRAM and NVSRAM based OXRAM at 180nm

Table 3. Comparison of 9T SRAM and 9T NVSRAM based OXRAM Performances

Performance Parameter	9T SRAM cell	NVSRAM based OXRAM
Technology	90nm	90nm
Transistor size	W=120nm, L=100nm	W=120nm, L=100nm
Voltage	0.7V	0.7V
Power consumption	10.5nW	9.8 nW
Leakage current	7.4nA	5.9nA
Delay	34.5ns	29ns

Table 3 results are shown in Figure 15. The graph indicates that at a supply voltage of 0.7, the values of power consumption, leakage current, and delay decrease with the NVSRAM-based OXRAM technique in comparison to 9TSRAM.

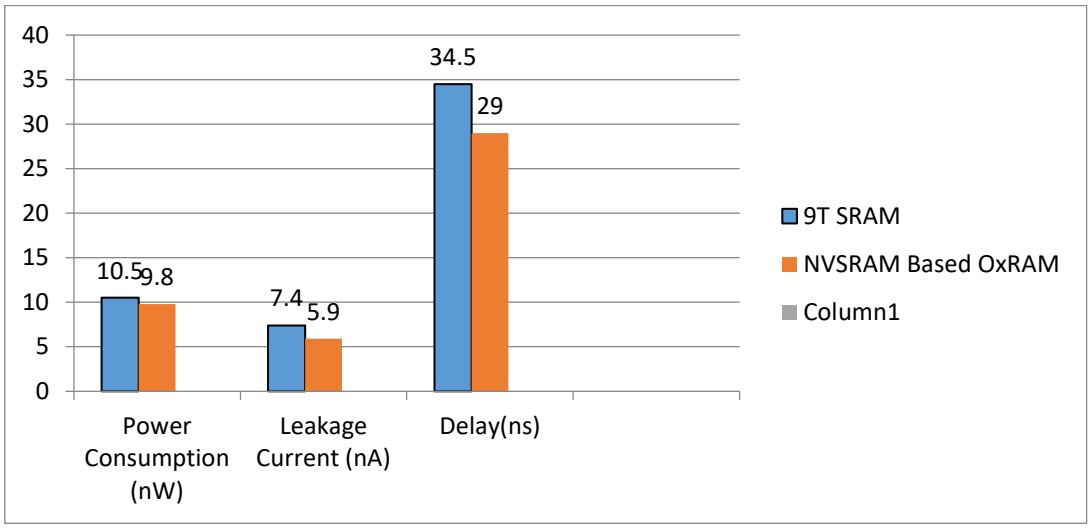

Figure 15. Graph Shows Comparison of 9TSRAM and NVSRAM based OXRAM at 90nm

Table 4. Comparison of Previous work with 9T NVSRAM based OXRAM Performances

References	Memory structure	Technology	Power supply	Power (When storing Data)	Current (When storing Data)
11	6T2R	130	1.8V	8.58mW	0-50µA
12	8T2R	280nm	0.9V	3.7nW	0-200µA
Proposed work	9TNVRAM	90nm	0.7V	3.5nW	0-40µA

Table 5. Comparison of Previous Work with Synapse SDSP

Performance Parameter	[13]	[14]	Synapse SDSP
Technology	55nm	180nm	90nm
Supply voltage	1V	1.8V	0.7V
Frequency	10Hz-350Hz	30Hz-1KHz	50Hz-1KHz
Energy per spike	1.099 nJ@10 Hz	883 pJ@30 Hz	2.52 nJ@50 Hz

Table 6. Comparison of Previous Work with 9T NVSRAM Cell

Performance Parameter	[15]	NVSRAM based OXRAM (180nm)	NVSRAM based OXRAM (90nm)
Voltage	0.6 V	1.8 V	0.7V
Power consumption	4.69µW	4.9 µW	0.098µW
Leakage current	9.32 µA	2.7µA	0.05µA

The graph indicates that at a supply voltage of 0.7, the values of power consumption and leakage current decrease with the NVSRAM-based OXRAM technique in comparison to 9TSRAM, as shown in Figure 16.

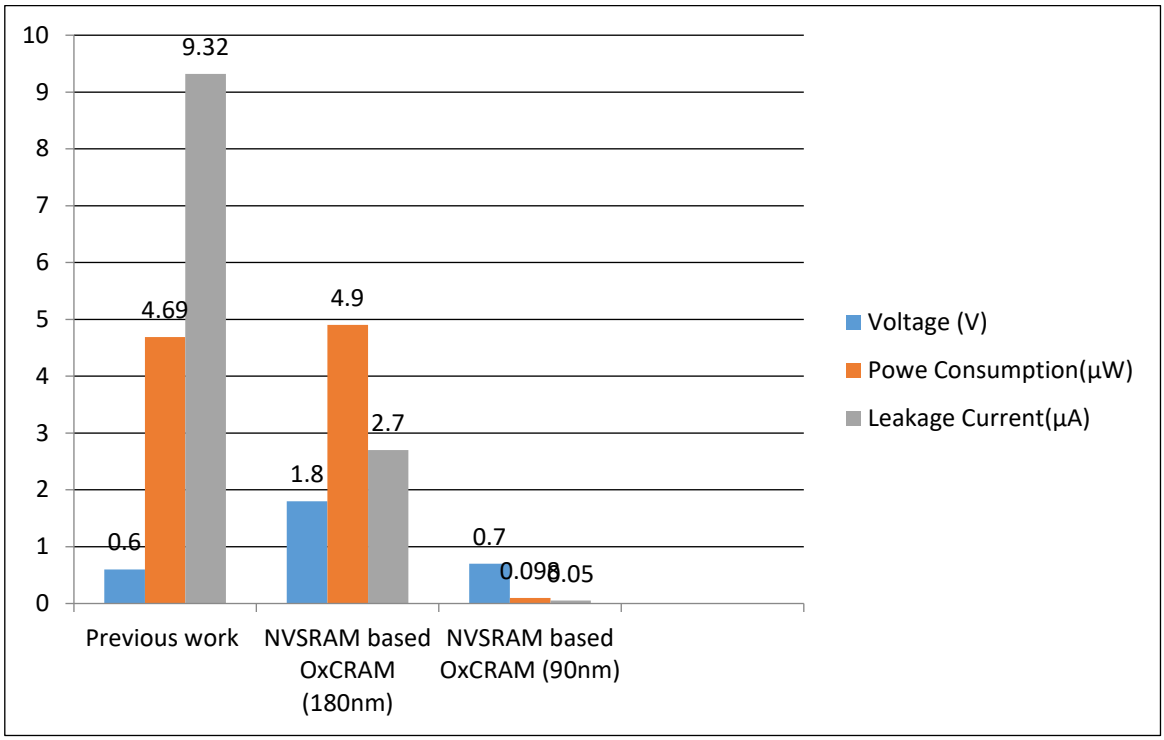

Figure 16. Graph Shows Comparison of NVSRAM based OXRAM at 90nm and NVSRAM based OXRAM at 180nm

4. Conclusion

In order to apply new memory, this article proposes an enhanced 9T NVSRCAM memory arrangement supported by the OXRAM technique. CMOS technology may be used with OXRAM to create non-volatile SRAM (NVSRAM) and other integrated circuits. The OXRAM technique is incorporated into the SRCAM to address the issue of information loss during a power outage. Prior to a power outage, the SRAM's data is saved in OXRAM. The issue of SRAM volatility is resolved while the power supply is restored since the data is moved back to SRAM. According to simulation results, the memory cell was created using 180nm and 90nm CMOS processes at 1.8 V and 0.7 V power supply voltages. It's reduced power dissipation and quicker information storage and reinstallation times, compared to earlier study findings, increase information storage stability. This study only confirmed the storage unit and tangential track designs from a functional standpoint, which had certain drawbacks. They emulated the NVSRAM. In order to make the design more favorable to the SRAM's read speed, we also need to take into account the influence of the forming process, as a degree of difference in arrangement necessitates an outline procedure prior to reading and writing, and the voltage required for this process is high. The majority of NVSRAM systems that utilize OXRAM technology store data in the far above-ground and near-to-ground resistance states of the memory. The SRAM and NVSRAM combination operate in a one-to-many mode because of this single mode. Nevertheless, studies have shown that OXRAM has the ability to store multiple values, meaning that a single OXRAM can hold several bits of data.

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