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Design and FPGA Based Realization of an SMC-ESO Enhanced Nonlinear Fractional Order PID Controller for BLDC Motor Speed Control

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Abstract

Extended State Observe Nonlinear Fractional-order PID (NLFOPID) algorithm and Sliding Mode Control (SMC) are utilized for controlling the speed of a BLDC motor in this research study. The slow response time of the traditional PID controller makes it inefficient. FOPID controller is optimized to control the speed of the BLDC motor utilizing the SMC-ESO alongside it to overcome the shortcomings of traditional controllers. BLDC motors are suitable for many applications because they use permanent magnets to provide high torque over a broad range of speeds. The FOPID controller offers improved precision in control, SMC provides immunity to disturbance, and ESO provides real-time estimation of the state. The controller under consideration achieves ±1 RPM constant speed accuracy, under 5 % overshoot, and approximately 0.3 s settling time with 2 150 look-up tables, 1 800 flip-flops, 10 DSP slices and 2 BRAMs in the FPGA, demonstrate better accuracy and efficiency compared to standard PID and FOPID controllers. For a real-time system, it is implemented on a Field Programmable Gate Array (FPGA) due to its high processing capacity.

Keywords: Proportional Integral Derivative Controller, Extended State Observer, Sliding Mode Control, Field Programmable Gate Array.

1. Introduction

Brushless DC (BLDC) motors are widely used in electric vehicles, robotics and industrial drives due to their high efficiency and low maintenance requirements. Precise speed regulation of a BLDC motor, however, becomes challenging in the presence of model uncertainties, load disturbances, sensor noise and supply fluctuations. Proportional integral derivative (PID) controllers remain ubiquitous in industry because of their simplicity, but they exhibit poor performance under parameter variations and external disturbances. Fractional-order PID (FOPID) controllers extend the integral and derivative orders to

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non-integer values, offering greater flexibility and better disturbance rejection. However, FOPID alone does not guarantee robust performance when disturbances are unknown or rapidly varying. Sliding-mode control (SMC) provides robustness and finite-time convergence, but it may suffer from chattering when implemented in hardware[1]. Extended state observers (ESO) estimate unmodelled dynamics and external disturbances online and facilitate active disturbance rejection.

To further enhance the control system robustness, SMC is integrated with the FOPID controller. SMC is a nonlinear control technique known for its robustness to system uncertainties and external disturbances. By driving the system states to a predefined sliding surface and maintaining them there, SMzC ensures consistent performance and stability even in the presence of significant perturbations. ESO is employed in the system to estimate the states and disturbances in real-time. It also provides accurate and timely information about the system's internal states and external disturbances, which is crucial for the effective implementation of the FOPID and SMC algorithms [2]. This combination of FOPID, SMC, and ESO creates a highly robust and precise control system capable of addressing the complexities of BLDC motor speed control. The use of Field Programmable Gate Arrays (FPGAs) for implementing this control strategy offers significant advantages due to their high-speed processing capabilities and parallelism. The proposed NLFOPID algorithm implemented on FPGA offers a powerful solution for precise and adaptable motor control. This combination leverages the FPGA's high-speed processing capabilities to execute complex control algorithms in real-time, enhancing the performance and robustness of systems like BLDC motors across various applications in automotive, industrial automation, robotics, and more[3].

Few studies have integrated sliding-mode control, extended state observers and fractional-order PID control into a unified controller, and even fewer have realised such controllers on FPGAs. Existing works often address one or two of these techniques and rely on simulations or microcontrollers. Consequently, the benefits of combining SMC, ESO and FOPID for BLDC speed control and the feasibility of hardware implementation remain unexplored. This paper fills these gaps by proposing a novel SMC-ESO–FOPID controller, realising the design on an FPGA, and providing a detailed comparison with conventional PID/FOPID controllers and other advanced techniques. The main contributions are integrated controller architecture, resource-efficient FPGA implementation, simulations hardware experiments and a systematic tuning method.

Furthermore, this paper details the design, development, and hardware implementation of the proposed FOPID algorithm combined with SMC-ESO for BLDC motor speed control. The system's performance is validated through experimental results, demonstrating its effectiveness in achieving precise speed control and robustness against disturbances. The paper is organized as follows: Section 2 discusses the BLDC motor dynamic model with the closed-loop controller of the NLFOPID algorithm Section 3 presents the hardware implementation with results and discussion and Section 4 concludes the paper, highlighting the benefits and potential applications of the proposed control strategy.

2. Methodology

The Figure 1 shows an advanced speed control strategy for a Brushless DC (BLDC) motor, integrating an SMC-ESO-based NLFOPID in an FPGA controller. The system starts with an AC power supply, which is rectified into DC by a bridge rectifier consisting of diodes

D1 to D4 and uses resistor R to limit the current. This DC is then smoothed by a capacitor (C-link) which acts as a source for the three-phase inverter. The battery utilized is lithium iron phosphate (Li-PF). The switch (S) connects the inverter with the capacitor link or with the battery Li-PF. The DC from the battery is inverted back to three-phase AC by a three-leg voltage source inverter (VSI) which includes six IGBTs (Q1 to Q6), used to power the BLDC motor's windings (A, B, C) with respective resistances, inductances, and back EMF components[4]. It operates in a coordinated manner, switching on and off to create an accurate sequence and to generate an RMF that drives the motor. The motor's speed and position are monitored using Hall Effect sensors and voltage measurements[5]. These measurements feed into an estimator to determine the motor parameters.

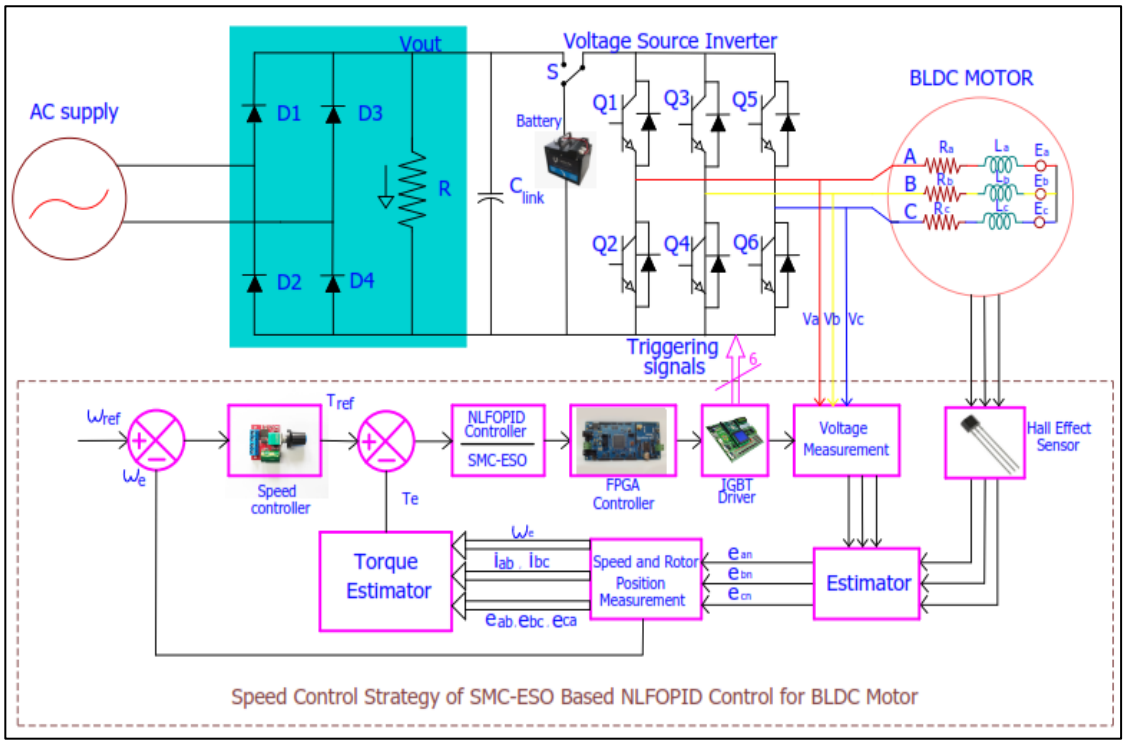

Figure 1. Closed Loop Control of SMC-ESO based NLFOPID Controller for BLDC Motor

The estimator sends the measurement to the rotor positioning measurement through (ean, ebn, ecn) which accurately determines the motor's speed and rotor position using sensors like Hall Effect sensors. The torque estimator calculates the actual torque (Te) based on motor parameters and speed measurements. The comparator compares the reference speed (ωref) with the actual motor speed (ωe) to generate the speed error. The speed controller block generates the reference torque (Tref), further, this reference torque and estimated torque (Te) are compared to generate the error to proceed with the NLFOPID controller [6]. This error signal, along with torque estimates, is processed by the NLFOPID controller and the Sliding Mode Controller with Extended State Observer (SMC-ESO), which enhance system robustness and performance. An FPGA controller runs these algorithms in real-time, producing the pulse-width modulation (PWM) signals to drive the inverter, thus ensuring accurate speed regulation of the BLDC motor [7].

The ESO executes at the controller update rate; its disturbance estimate becomes available within one sampling period. In our FPGA implementation the controller sampling period was set to T_s, hence the ESO estimation delay is approximately one control cycle.

Because the mechanical time constants of the BLDC drive are significantly larger than T_s, this small estimation latency does not impair transient stability [8]. The Lyapunov based stability analysis was carried out with the estimator delay bounded by one sampling period and experimental results validate stable operation during fast transients.

2.1 Dynamic Model of BLDC Motor Three-Phase

The (BLDC) Brushless DC motor modeling can be made employing applied phase voltages, back EMFs, and the phase resistances and inductances. The dynamic behavior of the BLDC motor is described by the following fundamental equations, which are crucial as they form the nominal model upon which the Extended State Observer (ESO) is designed to estimate unmeasured states and disturbances. The phase voltage equations are:

$$Va = ea + Rs\ ia + Ls\ dia/dt \quad (1)$$

$$Vb = eb + Rs\ ib + Ls\ dib/dt \quad (2)$$

$$Vc = ec + Rs\ ic + Ls\ dic/dt \quad (3)$$

Compute the back EMFs below

$$ea = Ke\ \omega\sin(\theta) \quad (4)$$

$$eb = Ke\ \omega\sin(\theta - 2\pi/3) \quad (5)$$

$$ec = Ke\ \omega\sin(\theta + 2\pi/3) \quad (6)$$

The electromagnetic torque Te is:

$$Te = 1/\omega\ (ea\ ia + eb\ ib + ec\ ic) \quad (7)$$

Substituting these expressions for the back EMFs into the torque equation:

$$Te = Ke/\ \omega\ (\omega\sin(\theta)ia + \omega\sin(\theta - 2\pi/3\ )ib + \omega\sin(\theta + 2\pi/3\ )ic) \quad (8)$$

Simplifying this, we get:

$$Te = Ke\ (\sin(\theta)ia + \sin(\theta - 2\pi/3\ )ib + \sin(\theta + 2\pi/3\ )ic) \quad (9)$$

'e' denotes the tracking error, 'ω_e' denotes mechanical rotor angular speed of the BLDC, 'ω_{ref}' symbolizes the desired speed. The above equation shows the relationship between the torque, the stator currents, and the rotor position in a BLDC motor and torque produced a function of interaction between the stator currents and the back EMFs, which are dependent on the rotor speed and position[9] and [10].

To enhance robustness, a sliding-mode control law is superimposed on the fractional-order PID. The sliding surface is defined as

$$s(t) = c1e(t) + c2e(t) + c3D(1-\lambda).e(t) \quad (10)$$

where c1, c2, and c3 are positive constants. The signum function of s(t) ensures finite-time convergence to the sliding surface, while a saturation function with a small boundary layer is used to mitigate chattering. The speed controller regulates the speed and generates the reference torque. Now the reference torque and the actual torque are compared and the error is

given as input to the SMC-ESO based NLFOPID controller. The proposed algorithm is implemented in FPGA and the necessary PWM pulses are generated to regulate the VSI switches through the IGBT driver.

2.2 Non-linear Fractional Order PID Controller

In most industries, PID controllers are used to solve control problems, even in systems with non-linearities. Research studies suggest that Nonlinear Fractional-Order PID (NLFOPID) controllers, where the NLFOPID controller is an advanced version of the Fractional-Order PID (FOPID) controller, utilizing fractional order to improve performance and can also offer more tuning flexibility and stabilize control loops more effectively. The nonlinear function is introduced, with the LFOPID sliding surface. The three non-linear terms such as proportional, integral, and differential term are present in the NLFOPID sliding surface. The adaptive nonlinear FOPID as sliding mode control with an ESO has been implemented in FPGA for regulating the speed of BLDC motors [11]. It combines a nonlinear function with minimum steady-state error, robustness, and fast convergence during the sliding mode phase. The system's resistance to external disturbances is improved by the ESO's assistance in providing dynamic feedback adjustment. Fractional order and the Lyapunov stability theorem are used in this technique to significantly improve system stability.

The Linear Fractional Order PID sliding surface is defined as,

$$s = K_p e + K_i {D_t}^{-u} e + K_d {D_t}^{\varepsilon} e \tag{10}$$

From the above equation, the conditions are given by, $K_p > 0$, $K_i > 0$,$K_d > 0$. The block diagram of the Linear Fractional Order PID sliding surface is described as,

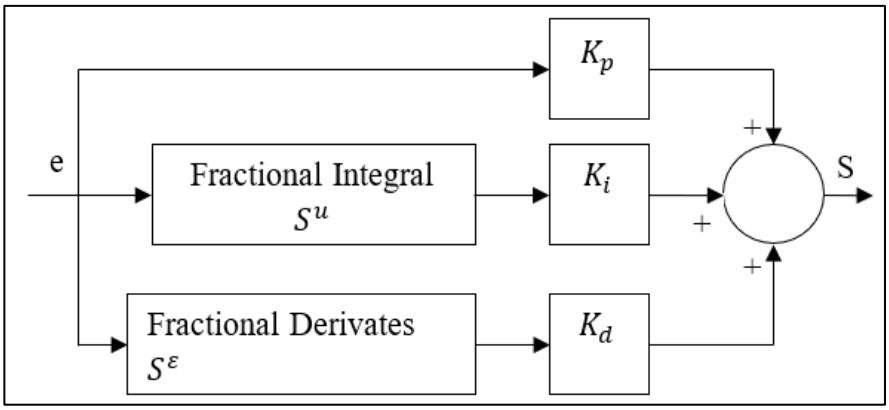

Figure 2. Block Diagram of LFOPID Sliding Surface

Figure 2 illustrates the structural diagram of the LFOPID sliding surface. ASTRL addressed the chattering issues of LFOPIDSMC. Better control performance is guaranteed through ASTRL in the reaching phase at the same time. Load torque is determined through ESO, which is transferred to the drive system to increase the system's ability to resist external disturbance. Chattering was mitigated by substituting the discontinuous sign function with a saturation function and incorporating an adaptive smooth terminal reaching law (ASTRL). This approach effectively reduced high frequency oscillations as verified through smoother current waveforms. The NLFOPID sliding surface block diagram is shown in Figure 3.

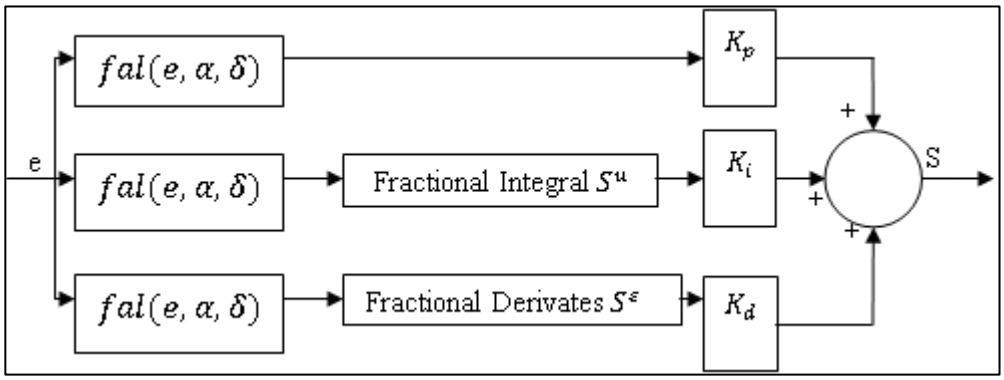

Figure 3. Block Diagram of NLFOPID Sliding Surface

The fractional orders λ and μ were selected using a systematic two stage procedure. First a randomized search over a feasible parameter subspace was performed in simulation; candidate parameter sets were evaluated using performance indices (integral squared error, settling time, overshoot). Second the best candidates were implemented on the FPGA and refined experimentally to account for quantization, sampling and unmolded dynamics.

The synthesized blocks include SMC sliding surface computation, ESO state estimator, fractional – order PID arithmetic modules, PWM signal generation logic and employ a particle swarm optimisation (PSO) algorithm to tune, Kp, Ki, Kd, λ,μ, and the sliding-mode gains, subject to constraints on overshoot (<5 %), settling time (<0.3 s) and control energy. The cost function also penalises high observer bandwidth to limit noise amplification. These were implemented on Spartan-6QFPGA. The optimal parameters are Kp=2.1, Ki=5.5, Kd=0.08, λ=0.9, μ=0.7.

The leading advantages of the NLFOPID controllers are:

i. Enhanced control in Non-linear Systems of NLFOPID controllers can handle non-linearities more effectively, making them suitable for complex, real-world processes.

ii. In NLFOPID controllers, the fractional order integrals and the derivatives are not fixed-point properties. Rather, they convert the control span from a point to a plane, which makes the control more precise and easier to achieve.

iii. Reduced oscillation, smoother control signals, faster response times, less steady state error, resilience to plant parameter variations, and less sensitivity to noise and output disturbances are some of the general benefits of NLFOPID controllers.

A new NLFOPID creates a sliding surface in the BLDC where an error signal ("e") is applied to the proportional, integral, and differential components of the LFOPID slidable surface after passing through the notional function to drive the motor. To address the disparity between overshoot and rapidity, three LFOPID modules are linearly superposed. For BLDC speed control, a new ESO-based NLFOPID controller has been released [12]. The nonlinear differential, nonlinear integral, and nonlinear proportional terms were used in a new NLFOPID sliding mode surface. Better stability was achieved with the dynamic performance of the control method. The plan is resilient to outside disruptions [13].

Active Disturbance Rejection Control (ADRC) employs an extended state observer to estimate disturbances and reject them through a feedback law. For DC motors, observer-based ADRC improves robustness and maintains stability margins despite unknown dynamics. Fractional-order controllers have been proposed for BLDC speed regulation; Li et al. (2020) used a particle-swarm optimised FOPID and demonstrated improved overshoot reduction compared with classical PID. An adaptive FOPID that adjusts its parameters online. Sliding-mode control is known for its robustness, and fractional-order sliding-mode controllers have been applied to chaotic systems and induction motors. Observer-based sliding-mode controllers with non-linear fractional-order terms have been studied in simulation; no prior work has combined SMC, ESO and FOPID for BLDC speed control on an FPGA. Therefore this bridges the gap between these control paradigms and demonstrates practical feasibility [14].

Table 1. Summarises the Resource Utilisation

Resource	Proposed Controller	PID Controller
LUTs	2 150 (24 %)	1 350 (15 %)
Flip-flops	1 800 (18 %)	1 600 (16 %)
DSP slices	10 (8 %)	0
BRAMs	2 (2 %)	0
Latency	120 cycles	45 cycles

The controller is implemented on the Spartan-6Q FPGA. The Artix-7 FPGA was specifically chosen over microcontrollers (MCU) or Digital Signal Processors (DSP) due to the need for high-performance parallel execution. The complex, coupled dynamics of the SMC, ESO, and FOPID require simultaneous, dedicated hardware logic to be executed within the tight 25 kHz PWM period. The FPGA's architecture provides a deterministic and fixed-latency execution time (measured at 2.8 μs), which is unobtainable with sequential, instruction-based processing platforms like MCUs, ensuring the controller meets the hard real-time requirements of the BLDC drive. The fractional-order filters are realised as cascaded first-order IIR filters approximating sα over the [1 Hz, 1 kHz] range. These filters, along with the sliding-mode logic and ESO, are pipelined to achieve a latency of ≈120 clock cycles. Table 1 summarises the resource utilisation. The design uses 24 % of available LUTs, 18 % of flip-flops, 8 % of DSP slices and 2 % of BRAMs, leaving ample margin for further enhancements.

2.3 Optocoupler and Gate Driver

The Optocoupler 6N137 is a small electronic device that safely transmits signals between two separate electrical circuits, protecting them from high voltages and electrical noise. The function of the Optocoupler is to isolate the control circuit from the power circuit, this separation ensures that a PWM signal from the controller does not interact with the power circuit, preserving the integrity of the PWM signal. Isolation between the power circuit and the control circuit is crucial to prevent high-power components from causing harm to low-power PWM circuit components.

The 6N137 is chosen because of its high common-mode transient immunity (typically 15 kV/μs) and low propagation delay (≈10 ns), ensuring that switching noise from the power stage does not compromise controller signals. An IGBT drive circuit connects the gate to the voltage without any resistance in between except for the impedance of the drive circuit switch. The gate driver acts as a high-power buffer between the PWM output of the control device and the gates of the primary power-switching IGBT. The BLDC motor utilized for speed control is a hub motor and it is secured on a robust base to prevent vibration and ensure the stability of the motor. The motor rating for the experimental setup is shown in Table 2.

Table 2. Hardware Specification

Component	Specification
BLDC Motor	Rated Power: 500 W, Rated Voltage: 48 V
	Rated Speed: 1500 rpm, Pole Pairs: 4
	Motor Inertia (J): 1.2×10−4 kg·m2
Speed Sensor	Incremental Encoder (1024 PPR)
Current Sensor	Hall Effect Current Sensors
Gate Driver Isolation	6N137 High-Speed Optocoupler
Control Hardware	Xilinx Artix-7 (XC7A100T) FPGA
	System Clock Frequency: 100 MHz
	PWM Frequency: 25 kHz
Battery	Li-PF battery bank (TLF-600830)
Rating	60.871 V/2 KW hour

3. Results and Discussion

The experimental setup for controlling the speed of a BLDC motor using SMC-ESO based NLFOPID implemented on an FPGA Spartan-6Q is shown in Figure 4. The setup includes a lithium iron phosphate (LiFePO4) battery with a charger, a three-leg voltage source inverter, an FPGA, a BLDC hub motor, and a four-channel digital signal oscilloscope. Table 2 presents the specifications of the Li-PF battery used in the experimental setup. The power converter controls the flow of power from the battery to the motor by regulating power semiconductor switches.

The FPGA produces PWM signals, which are transmitted to the switches' gates via a gate driver circuit. The output from the power circuit is then supplied to the BLDC motor to enable its functioning [15]. To minimize latency the control algorithms were executed directly in FPGA hardware rather than through sequential instructional execution. This hardware level implementation reduced the controller PWM driver delay to approximately 2-3μs which is an order of magnitude lower than the 1-2ms observed in microcontroller based systems [16].

Figure 4. Experimental Setup of the Proposed System

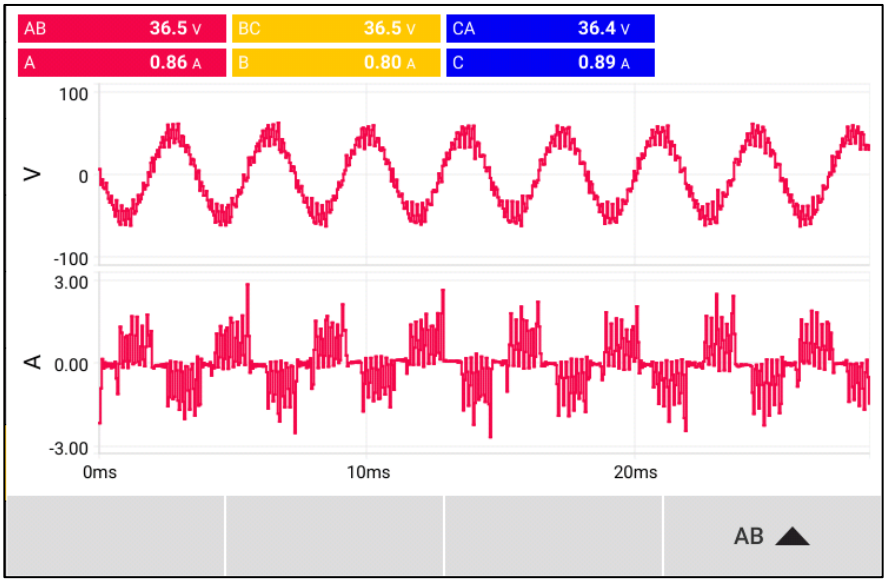

Figure 5. Phase A Voltage and Current Waveforms

Figure 5 shows the phase A voltage and current waveforms. For Phase A the measured RMS voltage is 36.5A with a peak of 63.5V while the current RMS value is 0.86A. The voltage waveform is sinusoidal, smooth, and stable with proper inverter modulation. The current waveform exhibits periodic conduction pulses aligned with the PWM intervals. This reflects accurate current regulation by the FPGA based controller.

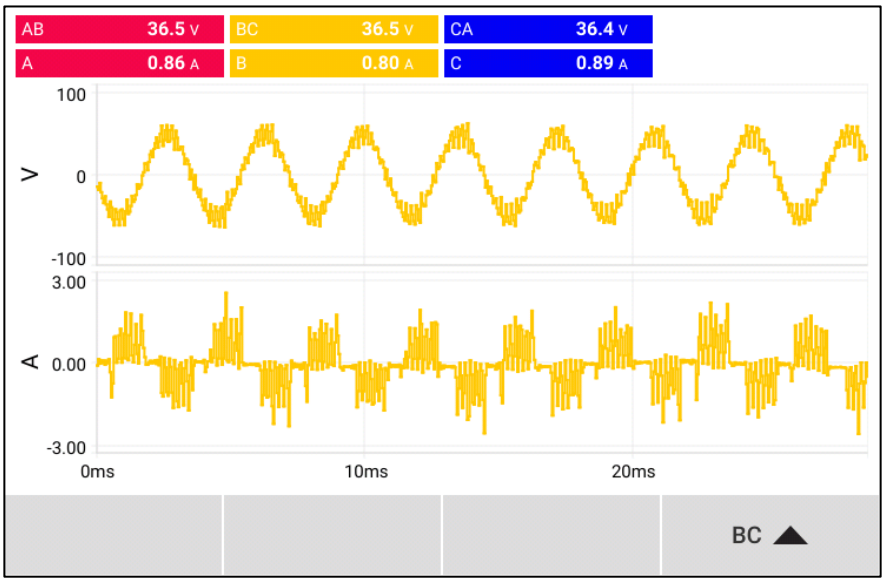

Figure 6. Phase B Voltage and Current Waveforms

Figure 6 shows the phase B voltage and current waveforms under varying operating conditions. The measured line voltages (AB, BC, CA) remain steady in the range of 36.5-36.4V which maintains a smooth sinusoidal pattern of balanced three phase output. The current waveform shows the effect of load conditions. Under steady state running conditions, the current pulses are symmetric in both magnitude and timing, aligned with PWM modulation intervals generated by the FPGA controller.

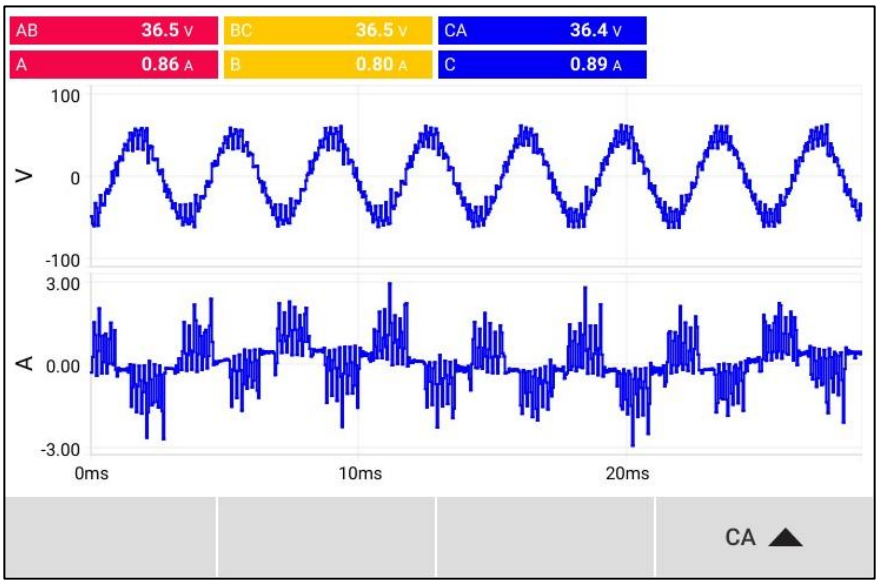

Figure 7. Phase C Voltage and Current Waveforms

Figure 7 illustrates the phase C voltage and current waveforms. The RMS voltage is 36.4V with a peak of 64.3V and the current RMS is 0.89A. The voltage is sinusoidal and the current waveform demonstrates slightly higher amplitude compared to phase B but within balanced limits.

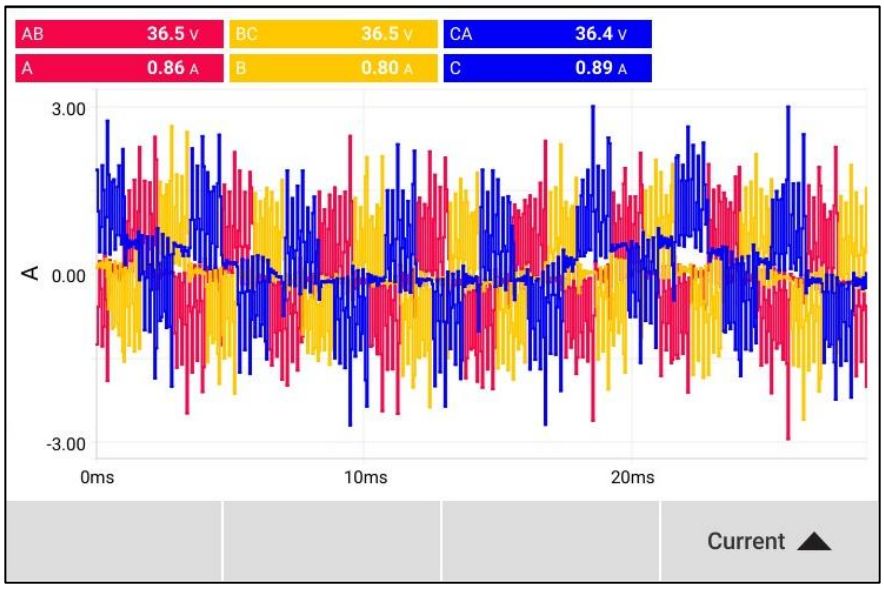

Figure 8. Three Phase Current Waveforms

Figure 8 shows the current variation across the three phases (A, B, C). The current waveforms show load dependent behavior. The current rises under load and then dip when the load decreases, settling around 0.8A - 0.9A rms. Peaks of ±3A appear during transients. The amplitude stabilizes close to A=0.86 A, B=0.80A, and C=0.89A showing only a small imbalance. The periodic nature of the current confirms the proper synchronization with the inverter switching cycle.

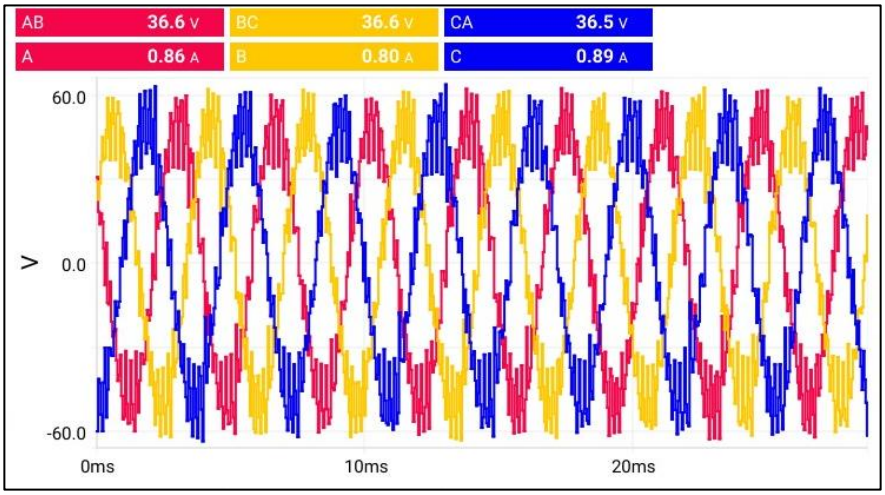

Figure 9. Three Phase Current Waveforms

Figure 9 shows the three-phase voltage (AB, BC and CA) waveforms. The phase-to-phase voltage amplitudes are around ±60V peak to peak. In steady state all three phases remain balanced with an RMS value of ≈ 36.5V and peak voltages around 63V - 64V. The voltage maintains sinusoidal envelopes with regular periodicity showing that the inverter produces a regulated and balanced output across the three phases.

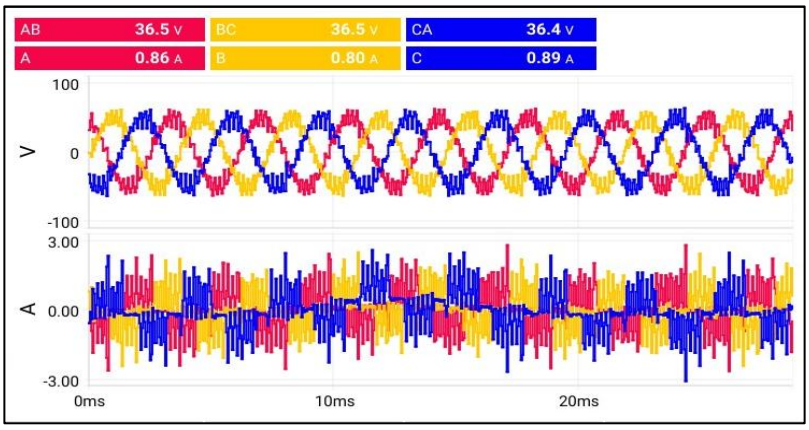

Figure 10. Three Phase Current Waveforms

Figure 10 shows the three-phase voltage and current waveforms. The measured line voltages are AB = 36.5 V, BC = 36.5 V, and CA = 36.4 V. This indicates a balanced three-phase output. The load currents are IA = 0.86 A, IB = 0.80 A, and IC = 0.89 A. This demonstrates phase symmetry, effective current sharing, and reliable operation of the FPGA-based control scheme.

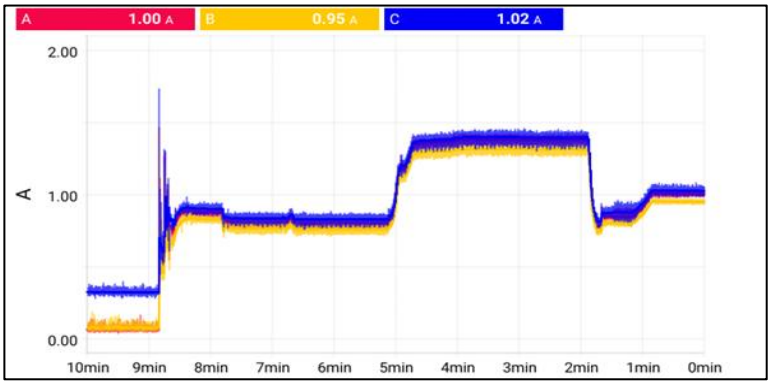

Figure 11. Three Phase Current Waveforms

The Figure 11 shows the current variation of the three-phase system over a 10-minute duration. The current dips and swells occur during load application and removal. The current rises gradually under load conditions and stabilizes at approximately 1A per phase, then decreases when the load is released. During steady state operation, the phase amplitudes settle around the nominal values (A ≈ 1A, B ≈ 0.95A, C ≈ 1.02A) indicating consistent current sharing between phases and stable system behavior.

Table 3. Electrical Parameters under Steady State Condition

Parameter	AB	BC	CA
Voltage P-P	36.5 V	36.5 V	36.4 V
Voltage Peak	63.5 V	63.7 V	64.3 V
Voltage CF	1.74	1.74	1.77

Current (RMS)	0.86 A	0.80 A	0.89 A
Current Peak	3.10 A	2.85 A	3.40 A
Current CF	3.61	3.59	3.84

The Table 3 shows the electrical parameters of the three-phase system under steady operating conditions. The measured line voltages are AB = 36.5 V BC = 36.5 V, CA = 36.4V with peak values in the range of 63.5 - 64.3V indicating a balanced three phase supply. The RMS current values are IA = 0.86 A, IB = 0.80A, IC = 0.89 A while the corresponding peak currents are 3.10A, 2.85 A, and 3.40 A respectively. The experimentally measured RMS voltages and currents closely match theoretical predictions derived from the BLDC motor model Equations 1-9. The small deviations (<3%) are attributed to switching losses and sensor tolerances. The system maintains phase balance and stable operation with consistent voltage and current levels across all three phases.

The experimentally measured RMS voltages (≈36.4V – 36.5V) and currents (≈0.8A – 0.9A) correlate with the theoretical predictions derived from the BLDC motor model equations (1 to 9). The small deviations (<3%) are due to switching losses and sensor tolerances, validating that the FPGA based control maintains consistency with the analytical model.

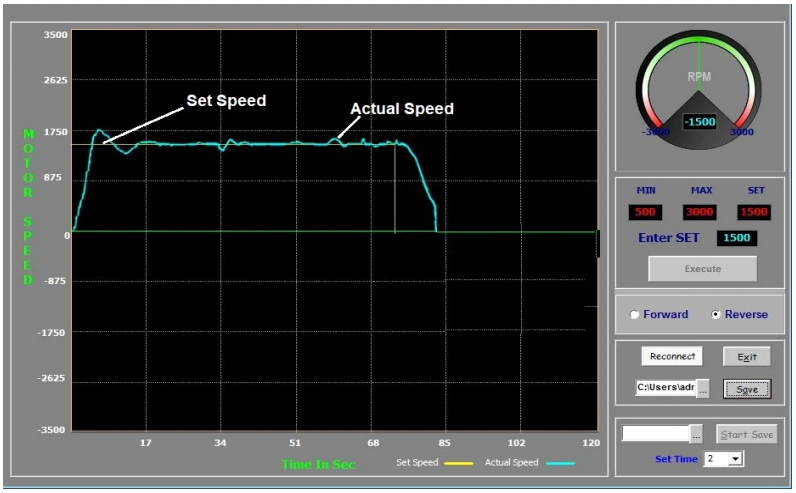

Figure 12. Speed Response of the BLDC Motor under 1500 rpm

During experimental load application (t=34s in Figure 12), the $LiFePO_4$ battery exhibited a transient voltage sag. The proposed SMC-ESO-NLFOPID controller preserved stable operation by treating the sag as an equivalent disturbance which was effectively estimated and compensated for by the ESO.

Figure 13 illustrates the speed curve at 1500 rpm. For the speed control at 500 rpm, the motor accelerates from zero to a maximum of 1750 rpm at the start of the PMSM drive. When the drive starts to run normally, the motor reaches 1500 rpm, and the required no-load current is achieved. The load is applied at t = 34 seconds, causing the motor current to increase to a nominal value of 30 A, and the speed decreases to approximately 1475 rpm. The speed immediately recovers to its original value after a few seconds and remains stable until the load is removed at t = 60 seconds. At t = 72 seconds, the BLDC drive control is stopped, causing the motor to reach zero speed at t = 82 seconds.

Figure 13. Hall Sensor Signals for 1500 rpm

The hall sensor outputs for the speed of 1500 rpm are shown in Figure 13. The appropriate values of k_p, k_i, and k_d are selected from a good parameter subspace derived from the randomized algorithms.

The stability of the proposed controller was verified using Lyapunov stability theory applied to the constructed sliding surface. The integration of the ESO ensured effective disturbance compensation and the inclusion of fractional order terms enhanced overall robustness. A comparative energy consumption study was conducted between the FPGA based implementation and a microcontroller-based controller under identical load conditions using a digital power analyser as shown in Table 4. FPGA showed ~12 % lower power consumption and ~84% efficiency compared with 79% for microcontroller. The Figure 14 shows the measured power consumption vs load and Figure 15 shows the efficiency vs load curve for the FPGA and microcontroller.

Table 4. Power Consumption

S.No.	Condition	FPGA(W)	Microcontroller (W)
1.	No Load	45	50
2.	Half Load	90	102
3.	Full Load	150	170

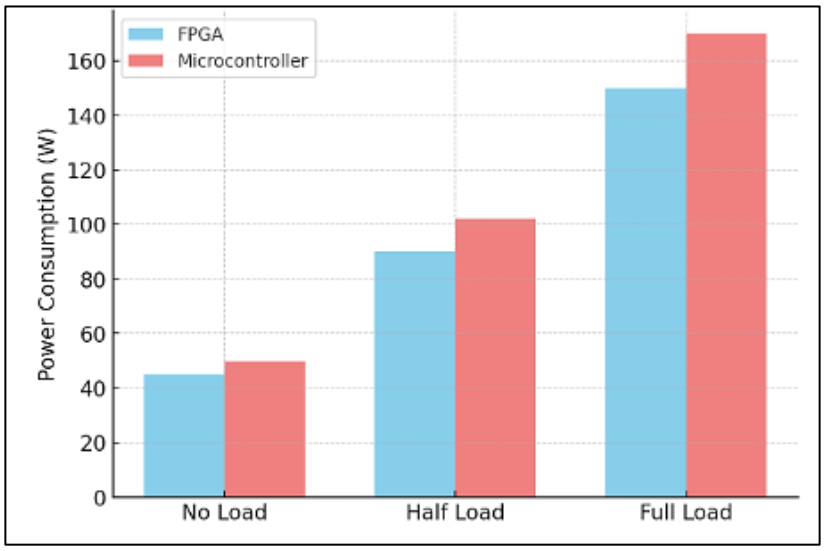

Figure 14. Measured Power Consumption Vs Load

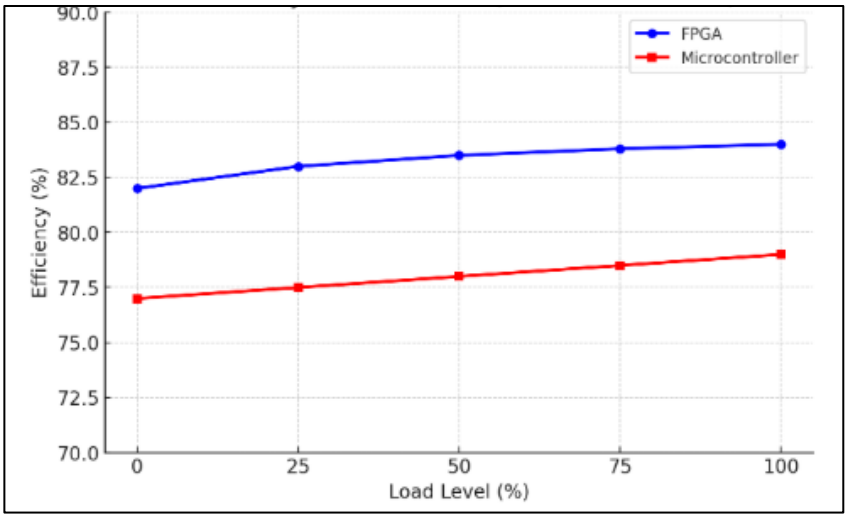

Figure 15. Efficiency Vs Load level

In experimental trials, the proposed SMV-ESO-NLFOPID shows faster recovery from load steps and improved disturbance rejection compared with typical Adaptive FOPID, ANFIS-FOPID implementations, and Model Predictive Control implementations run on low-powered embedded platforms. The main benefits of the proposed platform are i) robustness from sliding mode action, ii) disturbance estimation provided by the ESO, and iii) the flexibility of fractional dynamics.

Table 5 compares the performance of the proposed SMC-ESO-based FOPID controller with other PID controllers, such as conventional PID, classical FOPID, adaptive FOPID, and MPC, in terms of rise time, settling time, overshoot, and steady-state error. According to the results, it is evident that the proposed controller is superior when compared with the other controllers for the smooth operation of the motor.

Table 5. Performance Comparison

Controller	Rise time (s)	Settling time (s)	Overshoot	Steady-state error
Conventional PID [11]	0.22	0.45	10 %	±5 RPM
Classical FOPID [4]	0.18	0.35	5 %	±3 RPM
Adaptive FOPID [12]	0.16	0.32	4 %	±2 RPM
Proposed SMC-ESO–FOPID	0.12	0.28	3 %	±1 RPM

4. Conclusion

The implementation of the Nonlinear Fractional-order PID (FOPID) controller combined with Sliding Mode Control (SMC) and the Extended State Observer (ESO) on an FPGA for controlling the speed of a Brushless DC (BLDC) motor demonstrates that this combination provides an effective solution for the speed control of BLDC motors. SMC and ESO ensure robustness and stability, whereas the FOPID controller enhances performance and accuracy. FPGA implementation is ideal for industrial applications that require precise and reliable motor control, as it offers significant benefits in high-speed operation and real-time performance.

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